KU LEUVEN

ARENBERG DOCTORAL SCHOOL
Faculty of Engineering Science

Performance Optimization and Long Term Stability of Integrated GaN Diodes

Jie Hu

Supervisor:
Prof. dr. ir. G. Groeseneken

Dissertation presented in partial fulfillment of the requirements for the degree of Doctor of Engineering Science (PhD): Electrical Engineering

June 2016

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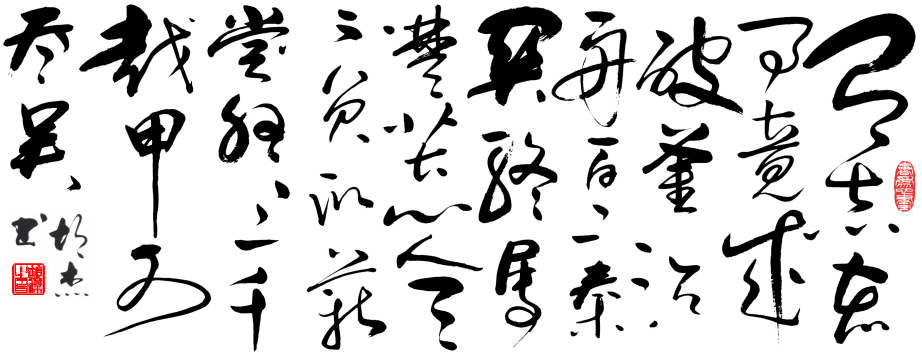
To my parents.



“Where there is a will, there is a way.”
“Wo ein Wille ist, ist auch ein Weg.”
“Waar een wil is, is een weg.”

Preface

As Bruce Lee says: "*All types of knowledge, ultimately mean self knowledge*." This PhD means more than accumulating and generating knowledge to me. Through this journey, I learned a lot and improved the awareness of my strengths and weaknesses. The acquired knowledge and improved self-perception in this process will be the invaluable treasure of my life. I would like to take this great opportunity to express my gratitude to those who helped me in the course of my PhD. Without your contributions, this thesis would not be possible and it won't be me.

First of all, I would like to extend my sincere gratitude to my promotor Prof. Guido Groeseneken who gave me the opportunity to start this PhD. Before that, I was firstly enrolled in the master program of nanoscience and nanotechnology in KU Leuven where Prof. Groeseneken was the program coordinator. Because of the inspirations I gained from his lectures, I was determined to work on reliability of power devices. I was so lucky to be offered with this exciting PhD topic under his supervision. Throughout the past 4 years, he has been always supportive of my research activities and giving me great freedom to pursue new ideas. His philosophy of "learning by doing and teaching" inspires me to challenge myself in a very different fashion. I am indebted to him for his great support, encouragement and supervision.

Dr. Steve Stoffels (imec) as my daily-supervisor deserves special thanks for always being supportive of my work and helping me embed myself in the GaN team at imec. I appreciate his scientific criticism, experience and knowledge, various perspectives on many topics, and his efforts to arrange regular meetings with me no matter how busy he is. He is very kind and always open for new discussions. I am grateful for the collaborations we had throughout this PhD and his help to obtain many of the results in this thesis.

Special thanks to the other PhD committee members: Prof. Johan Driesen (KU Leuven), Prof. Marc Heyns (imec and KU Leuven), Prof. Benoit Bakeroot (imec and Ghent University), Dr. Clemens Ostermaier (Infineon Technologies Austria AG), and Prof. Jean Berlamont (KU Leuven). Thanks for their kind perusal of the manuscript and the valuable comments on my manuscript to improve the quality of this thesis.

This thesis would not be possible without continuous support from the imec GaN team. Dr. Stefaan Decoutere, as the GaN program director, deserves my gratitude in many aspects. His experience in the field, insights and decision-making skills are impressive. It is my great fortune to have him as my boss who trusted me and trained me with wide perspectives. Next to that, I would like to acknowledge the help from Dr. Silvia Lenci and ir. Brice De Jaeger as the process integration engineers. They two helped me to process many interesting samples and learned me a lot about the process details.

As a characterization engineer in the group, I would like to extend my gratitude to Dr. Nicoló Ronchi, Dr. Rafael Venegas, and Xuanwu Kang. I enjoyed working with you in the lab and learned a lot from you. I would like to also thank the following GaN team members: Tian-Li Wu, Vice Sodan, Dr. Shuzhen You, Karen Geens, Dr. Niels Posthuma, Dr. Marleen Van Hove, Dr. Dirk Wellekens. Moreover, I would like to thank Andrea Natale Tallarico (University of Bologna) for the nice work we collaborated.

I would like to acknowledge the strong support from the Epi-GaN team at imec. Thanks to Dr. Yoga Saripalli, Dr. Ming Zhao, Dr. Hu Liang, and Dr. Prem Kumar Kandaswamy for your achievements. Without your contributions, I will end up with pure TCAD simulations. It is you who gave me the foundation to build up my thesis work.

In 2015, I had the opportunity to perform research at Massachusetts Institute of Technology (MIT) to expand my horizons. I would like to thank Prof. Tomás Palacios for hosting me. Many thanks to the nice people I met or worked with at MIT: Prof. Jesús Grajal de la Fuente, Dr. Marco de Fazio, Dr. Puneet Srivastava, Dr. Amirhasan Nourbakhsh, Dr. Noelia Vico Triviño, Dr. Ujwal Radhakrishna, Min Sun, Yuhao Zhang, Daniel Piedra, Sameer Joglekar, Elaine McVay, Marek Hempel, Wenjie Lu, Yufei Wu, etc. This experience forms a special component in the course of my PhD and it is unforgettable. I would like to also acknowledge the financial support from the National Fund for Scientific Research (FWO) of Belgium to make this possible.

The past four years at imec have been great fun for me, big thanks to my colleagues/ex-colleagues, and friends who helped me: Dr. Leqi Zhang, Yi Ren, Dr. Yi Li, Dr. Daniele Leonelli, Irene Kwee, Markus Heyne, Frank Vleugels, Dr. Ming Zhao, Dr. Hu Liang, Dr. Denis Lin, Dr. Andrea Firrincieli, Tian-Li Wu, Dr. Yan Li, Abhitosh Vais, Dr. Song Liu, Dr. Attilio Belmonte, Dimitrios Andrikopoulos, Elena Capogreco, Michael Chen, Dr. Andrea Fantini, Erik Bury, Dr. Geert Hellings, Dr. Ben Kaczer, Dr. Arturo Sibaja-Hernandez, Devin Verreck, Murad Redzheb, Prof. Eddy Simoen, Sathish Kumar Dhayalan, Mikhail Krishtab, Prof. Valeri Afanasiev, Dr. Sergiu Clima, Augustin Lu, Cesar Javier Lockhart de la Rosa, Dr. Dries Dictus, Suseendran Jayachandran, Sebastien Moitzheim, Brecht Put, Pavlo Fesenko, Manoj Nag, Dr. Ajay Sampath, Yue Pan, Dr. Tung Huei Ke, Dr. Kai Cheng, Dr. Sijia Jiang, Dr. Liyang Zhang, Dr. Hongyu Yu etc.

As a member of the Chinese community, I would like to thank my friends and Chinese fellows who I made acquaintances or worked with. They are: Dr. Leqi Zhang, Dr. Yi Li, Dr. Yan Li, Dr. Song Liu, Yi Ren, Dr. Sijia Jiang, Dr. Mingxu Liu, Dr. Chang Chen, Dr. Bo Wang, Dr. Shuzhen You, Dr. Yangyin Chen, Dr. Baojun Tang, Dr. Xiaojie Chen, Dr. Wen Fang, Dr. Peter Tseng, Dr. Tung Huei Ke, Dr. Lianggong Wen, Dr. Ming Mao, Xiangyu Wu, Enlong Liu, Xubin Chen, Weiming Qiu, Ziyang Liu, Chen Wu, Xu Han, Qixian Shi, Prof. Dixian Zhao, Hao Yu, Menglei Xu, Xiangdong Li, Dr. Yuyi Wang (ETHZ), Dr. Bo Gao, Jingdong Yan, Dr. Jiaqi Li, Jigang Ma, Dr. Yunlong Li, Dr. Hu Liang, Dr. Xiaoping Shi, Dr. Ming Zhao, Dr. Weimin Gao, Dr. Weiming Guo, Dr. Teng Wang, Dr. Liu Yang, Shengping Mao, Jia Shi , Liping Zhang, Dr. Lei Zhang, Yiting Sun, Hongtao Chen, Haodong Zhang, Yuandong Li, Yan Cai, Riqing Zhang, Zheng Chai, Yue Pan, Jia Chen, Dun Mao, Yiming Yang, Yanan Hu,

Lai Wei, Ding Yuan, Xiao Liu, Luman Zhang, Danna Xin, Fan Yang, Yixin Cai, Yusi Chen, Fan Zhang (MIT, HKUST), Yuzhu Gai (NXP), Gaozhan Cai, Yi Hou, Liang Su, Junjie Yi, Zhang Wang, etc.

Finally, this book is dedicated to my beloved parents Jianming Hu and Meili Yan. Thanks for your deepest love and endless support. The greatest appreciation goes to my wife, Xinyu Zhou, thanks for your care, understanding, trust, and love. I could have never come to this stage without your support. Thank you, I love you all.

Jie Hu

June 2016

Leuven, Belgium

Abstract

Power electronics are used in advanced technology for generating and using sustainable energy. Examples are solar converters, motor drives, hybrid electrical vehicles or switch mode power supplies. In this technology, they play a key role in any form of power conversion. Gallium Nitride (GaN), next to its use in light emitting diodes (LEDs), also enables high-voltage, high-power, and high-temperature electronic circuits. It has an electrical breakdown field that is an order of magnitude higher than silicon. The AlGaN/GaN materials system offers significant advantages over Si for power devices, as it allows fabricating High-Electron-Mobility Transistors (HEMTs) with fast switching properties, high ratio of breakdown voltage over on-resistance, and high temperature operation. In power convertors, the circuits usually require a high voltage power diode next to the HEMT transistor.

The purpose of this PhD is to look into the fundamental aspects of the design of GaN diodes, and the process architectures for co-integration with the HEMT. This thesis shows that the AlGaN/GaN Schottky barrier diode with a gated edge termination (GET-SBD) proves to be a promising architecture. Combined with AlGaN barrier recess process in GET-SBD, low leakage current and low forward voltage can be simultaneously achieved in GaN diodes demonstrating state-of-the-art performance. This has been experimentally realized in small GaN diodes and 10-mm power diodes, fabricated on 8-in silicon wafers with Au-free CMOS-compatible process flows. However, the stability of the forward characteristics can be severely influenced by electron trapping, when the GaN diode is subjected to off-state stress.

Significant improvement in diode stability has been achieved by applying plasma cleaning steps, using an *in-situ* SiN passivation layer and low-dispersive buffer layers, etc. Initial reliability tests show that the GET-SBD has a good on-state reliability. Sequential time-dependent dielectric breakdown characteristics have been observed when GET-SBDs were stressed in high temperature reverse bias (HTRB) reliability tests. In summary, the low-cost recessed GET-SBD architecture has demonstrated competitive performance over Si and SiC power diodes for 200-V application platform, further buffer design and better choice of the edge termination materials are required to allow for stable and reliable GaN diodes towards higher voltage applications.

Zusammenfassung

Gallium Nitrid (GaN) kann neben seiner Verwendung in Leuchtdioden (LEDs) ebenfalls in Hochvolt-, Hochleistungs- und Hochtemperaturschaltkreisen eingesetzt werden. GaN hat eine elektrische Durchbruchsfeldstärke, die eine Größenordnung über der von Silizium liegt. AlGaN/GaN Materialsysteme besitzen beträchtliche Vorteile gegenüber Silizium-basierter Leistungselektronik, da mit AlGaN/GaN Transistoren mit hoher Elektronenmobilität (HEMTs) und schnellen Schaltverhalten hergestellt werden können. Diese zeichnen sich durch ein hohes Verhältnis zwischen Durchbruchspannung und AN-Widerstand aus und können auch bei hohen Temperaturen eingesetzt werden. In Leistungswandlern werden neben HEMT Transistoren auch Hochvolt-Leistungsdioden verwendet. Das Ziel dieser Arbeit ist die Erforschung fundamentaler Aspekte des Designs von GaN Dioden und der Prozessarchitektur für die Kointegration mit HEMTs. Diese Arbeit stellt AlGaN/GaN Schottky-Dioden mit modulierbarer Seitenterminierung (GET-SBD) als eine vielversprechende Architektur vor. Durch die Kombination mit dem AlGaN Barrieren-Recess-Prozess können gleichzeitig geringe Leckströme und niedrige Vorwärtspannungen erzielt werden. Dazu wurden kleine GaN Dioden und 10-mm Leistungsdioden auf 200 mm Siliziumwafern mit Gold-freien, CMOS-kompatiblen Prozessen hergestellt. Jedoch wird die Stabilität der Vorwärts-Charakteristik entscheidend durch Elektronentrapping beeinflusst, bei welchem die GaN Diode Stress ausgesetzt ist. Eine entscheidende Verbesserung in der Diodenstabilität wurde durch die Anwendnung von Plasma Reinigungsschritten, einer *in-situ* SiN Passivierungsschicht und niedrig dispersiven Pufferschichten erreicht. Erste Untersuchungen haben eine gute Zuverlässigkeit im AN-Zustand demonstriert. Aufeinanderfolgende, zeitabhängige Dielektrik Durchbruch-Eigenschaften wurden in den GET-SBD Architekturen durch Hochtemperatur Reverse-Bias Zuverlässigkeitsuntersuchungen (HTRB) erforscht. Die kostengünstige GET-SBD Architektur hat konkurrenzfähige Performance gegenüber Si und SiC Leistungsdioden für 200 V Anwendungsplattformen gezeigt. Weitergehend sind das Design der Pufferschichten und die Wahl des Materials für die Randterminierung entscheidend, um stabile und zuverlässige GaN Dioden für Hochvolt-Anwendungen herzustellen.

Samenvatting

Gallium nitride (GaN) biedt, naast het gebruik in licht-emitterende diode (LEDs), ook de mogelijkheid om elektronische circuits te realiseren voor hoge spanningen, hoge vermogens en een hoge temperatuurswerking. Het materiaal heeft een elektrische doorslagveldsterkte die een orde groter is dan deze van Silicium. De AlGaN/GaN materiaalcombinatie biedt veelbetekende voordelen ten opzichte van Si betreffende vermogensscomponenten, aangezien het toelaat om veldefffecttransistoren (type High-Electron-Mobility Transistors (HEMTs)) te vervaardigen met snelle schakeleigenschappen, hoge verhouding van doorslagspanning op "aan-weerstand", en hoge temperatuurswerking. In omvormers vereisen de schakelingen doorgaans, naast de HEMT transistor, een hoogspanningsdiode.

Het doel van dit doctoraatsonderzoek is het bestuderen van de fundamentele aspecten van het ontwerp van de GaN diodes, en het fabricatie procedé voor de co-integratie met de HEMT. Deze thesis toont aan dat de AlGaN/GaN Schottky diode met een gecontroleerde diëlektrische terminatie "gated edge termination" (GET-SBD), de meest belovende architectuur is. Gecombineerd met een AlGaN verdunning procedé in de GET-SBD, kan gelijktijdig zowel een lage lekspanning als een lage doorlaatspanning gerealiseerd worden, waardoor state-of-the-art performantie bereikt wordt. Dit werd experimenteel gerealiseerd in kleine GaN diodes en 10-mm vermogensdiodes, gefabriceerd op 8-inch silicium wafers met een Au-vrij CMOS-compatibel fabricatie procedé. Echter, de stabiliteit van de doorlaatkarakteristieken kan sterk beïnvloed worden door het opnemen van elektronen in het materiaal, wanneer de GaN diode onderworpen is aan een stress conditie in de af toestand van de component.

Beduidende verbetering in de diode stabiliteit werd bereikt door het toepassen van plasma reiningstappen, *in-situ* SiN passivatie laag, lage-dispersieve buffer lagen, etc. Initiële betrouwbaarheidstests tonen aan dat de GET-SBD een goede betrouwbaarheid bezit, wanneer de component in de aan toestand gestuurd wordt. Sequentiële tijdsafhankelijke diëlectrische doorslagkarakteristieken werden waargenomen wanneer de GET-SBDs aan betrouwbaarheidstesten onderworpen werden met hoge temperatuur en negatieve spanning "high temperature reverse bias" (HTRB). Samengevat, de lage kost GET-SBD architectuur met het verdunningsprocedé heeft competitieve performantie aangetoond ten opzichte van Si and SiC diodes voor 200-V toepassingen platform. Verder buffer ontwerp en een betere keuze van de materialen voor de terminatie van de diode zijn vereist om stabiele en betrouwbare GaN diodes te bekomen voor toepassingen met hogere spanning.

Table of Contents

List of Abbreviations

Acronym	Description
2DEG	Two-Dimensional Electron Gas
AC	Alternating Current
ALD	Atomic Layer Deposition
ALE	Atomic Layer Etching
BD	Break Down
BV	Breakdown Voltage
CC	Current Collapse
CMOS	Complementary Metal-Oxide-Semiconductor
C-V	Capacitance-Voltage
CVS	Constant Voltage Stress
DC	Direct Current
DD	Dislocation Density
DH	Double Heterostructure
EET	External Edge Terminated
EET-SBD	External Edge Terminated Schottky Barrier Diode
E-Field	Electric Field
EMI	Electromagnetic Interference
ET	Edge Termination
FP	Field Plate
FOM	Figure-of-Merit
GET	Gated Edge Termination
GET-SBD	Gated Edge Terminated Schottky Barrier Diode
GIXRD	Grazing Incidence X-Ray Diffraction
IMEC	Interuniversity MicroElectronics Centre
IMP	Ionized Metal Plasma
LED	Light Emitting Diode
L-FER	Lateral Field Effect Rectifier
HEMT	High Electron Mobility Transistor
HEV	Hybrid Electrical Vehicle
HTRB	High Temperature Reverse Bias
I-V	Current-Voltage
MBE	Molecular Beam Epitaxy
MIS	Metal-Insulator-Semiconductor
MISHEMT	Metal-Insulator-Semiconductor HEMT
MIT	Massachusetts Institute of Technology
MOCVD	Metal Organic Chemical Vapor Deposition
MOS	Metal-Oxide-Semiconductor

Acronym	Description
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MS	Metal Semiconductor
MSM	Measure-Stress-Measure
PEALD	Plasma-Enhanced Atomic Layer Deposition
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PC	Personal Computer
PV	Photovoltaic
PVD	Physical Vapor Deposition
PWM	Pulse Width Modulation
RESURF	Reduced Surface Field
RF	Radio Frequency
RTA	Rapid Thermal Annealing
RTCVD	Rapid Thermal Chemical Vapor Deposition
SBD	Schottky Barrier Diode
SBH	Schottky Barrier Height
SC	Schottky Contact
SEM	Scanning Electron Microscopy
SILC	Stress Induced Leakage Current
SIMS	Secondary Ion Mass Spectrometry
TAT	Trap Assisted Tunneling
TCAD	Technology Computer-Aided Design
TDDB	Time-Dependent Dielectric Breakdown
TE	Thermionic Emission
TEM	Transmission Electron Microscopy
TLM	Transmission Line Model
TP	Trap
TU	Tunneling
UID	Unintentionally Doped
WBG	Wide Band Gap
WF	Work-Function
WKB	Wentzel Kramer Brillouin
XRD	X-ray Diffraction
XPS	X-ray Photoelectron Spectroscopy

List of Symbols

Symbol	Unit	Description
A^*	A/mm^{2}K^2	Richardson Constant
β	-	Weibull Slope
η	-	Scale Parameter
ϵ_r	F/m	Relative Permittivity of Semiconductor
E_critical	V/m	Critical Electric Field
ΔE_C	eV	Conduction Band Energy Offset
ΔE_V	eV	Valence Band Energy Offset
E_C	eV	Conduction Band Energy
E_F	eV	Fermi Energy Level
E_g	eV	Semiconductor Band Gap
E_t	eV	Tunneling Energy
E_T	eV	Trap Energy Level
E_V	eV	Valence Band Energy
ϕ_m	eV	Metal Work-Function
χ	eV	Electron Affinity
F(t)	-	Cumulative Density Function
$f(t)$	s^{-1}	Probability Density Function
σ_n	cm^2	Capture Cross-Section
λ	cm	Tunneling Attenuation Constant
λ(t)	-	Failure Rate or Hazard Rate
I_{ON}	A/mm	ON-state Current
I_{OFF}	A/mm	OFF-state Current
J_t	A/cm^2	Tunneling Saturation Current
k_b	$m^2kgs^{-2}K^{-1}$	Boltzmann Constant
L_AC	μm	Anode-to-Cathode Spacing
L_G	μm	Length of Edge Termination
L_SC	μm	Length of Schottky Contact
L_SDG	μm	Spacing between the Schottky Contact and the External Edge Termination
μ_n	cm^2/Vs	Electron Mobility
n	-	Ideality Factor
N_D	cm^{-3}	Doping Concentration
N_dis	cm^{-2}	Dislocation Density
Φ_B	eV	Schottky Barrier Height
Φ_{MS}	eV	Metal-to-Semiconductor Workfunction Difference
P_ON	W	ON-state Power Loss

Symbol	Unit	Description
P_{OFF}	W	OFF-state Power Loss
P_{PZ}	C/m^2	Piezoelectric Polarization
P_{SP}	C/m^2	Spontaneous Polarization
q	C	Elementary Charge
ρ	$\Omega \times$ m	Resistivity
ρ_{pol}	C/m^2	Polarization Charge Density
R_C	$\Omega \times$ mm	Contact Resistance
R_{ON}	Ω	ON-Resistance
$R_{ON,sp}$	$\Omega \times$ m^2	Specific ON-Resistance
R(t)	-	Reliability Function
σ_p	C/m^2	Polarization Charge Density
T	K	Absolute Temperature
τ	s	Time Constant
ν_D	s^{-1}	Debye Frequency
V_F	V	Forward Voltage
V_{OFF}	V	OFF-State Voltage
V_{ON}	V	ON-State Voltage
V_R	V	Reverse Voltage
V_T	V	Diode Turn-On Voltage
V_{TH}	V	MISCAP/MISHEMT Threshold Voltage
W_D	μm	Depletion Width

Chapter 1

Introduction

1.1 Advanced Power Electronics

Power electronics is the branch of electronics dealing with the efficient conversion and control of electrical power by means of electronic switching devices. Specific applications range from switch mode power supplies to solar converters, wind turbines, motor drives, hybrid electrical vehicles (HEVs), etc. As is shown in Figure 1.1, different voltage and current ratings are required according to the specific application[1]. In these applications, power converters (DC/DC, AC/DC, AC/AC converters and DC/AC inverters) are widely used. The electronic devices in the converters play an essential role to allow for the power conversion and the improvement of energy conversion efficiency.

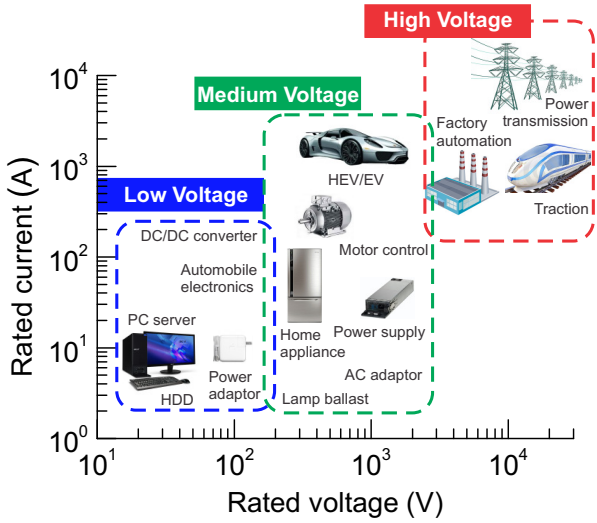


Figure 1.1: Specific applications with different voltage and current ratings.

[1] At current stage, GaN lateral power devices are targeting at "Low Voltage" (i.e. 200 – 650 V) applications. The limiting factors for higher voltage applications of lateral GaN devices are related to parasitic buffer or dielectric breakdown. Vertical GaN diode, based on bulk GaN substrate, can already reach breakdown voltage as high as 3.7-kV [1].

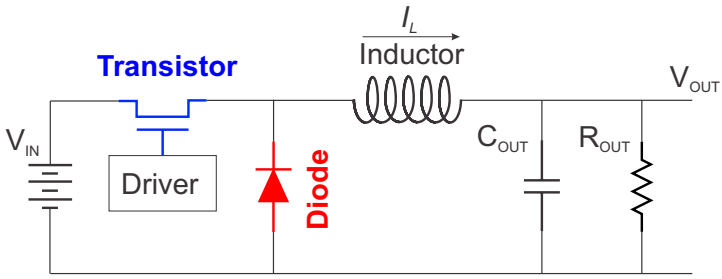


Figure 1.2: The circuit schematic of a simplified buck converter which allows for the down-conversion of DC voltages.

1.1.1 Energy Saving with Efficient Power Devices

Figure 1.2 shows the circuit schematic of a simplified buck converter which can be used for the down-conversion of DC voltages (high input voltage to low output voltage). The power transistor and diode in the converter are used as the switching devices combining with inductor, capacitor, and resistor as the passive components to deliver required output voltage under certain switching conditions. To enable efficient power conversion from the input to the output, the electronic components in the converter should dissipate minimal energy. The power loss of the electronic components in a switching circuit has two parts: dynamic power loss and static power loss. The dynamic power loss occurs when the device switches from ON-state to OFF-state or vice versa. Unipolar devices are preferred to lower the dynamic power dissipation due to their fast switching capability and low recovery current. The static power loss is connected to the operating point. In Figure 1.3, the comparison of ideal and real *I*–*V* characteristics for transistor and diode is presented. In the ideal case, the transistor and diode deliver infinite current in on-state with no voltage drop and block the current completely with any reverse voltage applied. In reality, some ON-state voltages are needed for transistor (V_{DS}) and diode (V_{F}) to pass on-state currents through the devices. In the OFF-state, the transistor drain-source leakage and diode leakage currents are inevitable at high reverse bias. Furthermore, the devices can break down at certain reverse bias (i.e. BV: breakdown voltage) and lose their blocking capability and device function. The practical operation of the devices in converters can result in unavoidable power loss. The static power loss can be described as:

$$P_{static} = P_{ON} + P_{OFF} = V_{ON} \times I_{ON} + V_{OFF} \times I_{OFF}, \tag{1.1}$$

where both ON-state and OFF-state operations contribute to the energy dissipation in the devices. It is important for the device engineer to design power devices with low ON-state voltages (or low R_{ON}) and low OFF-state leakage currents. Furthermore, the breakdown voltage (BV) should be designed higher than the rated voltage with

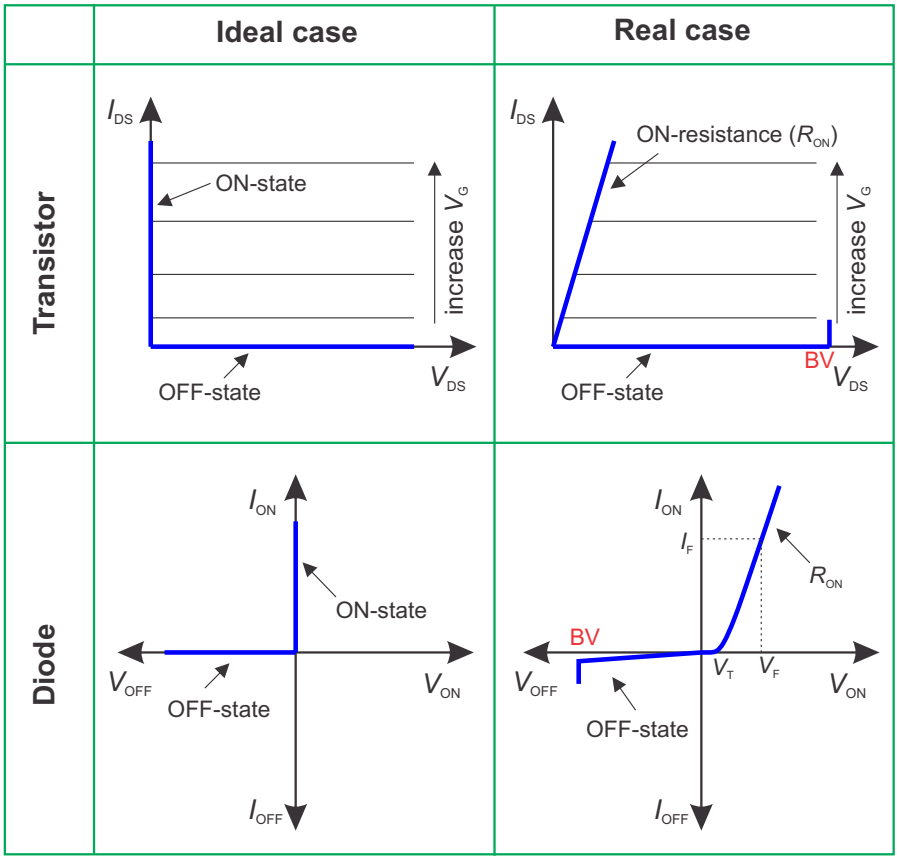


Figure 1.3: Schematics of the ideal and real *I*–*V* characteristics for transistor and diode in OFF- and ON-state [2].

sufficient margin. However, the OFF-state BV and ON-resistance (R_{ON}) of unipolar devices cannot be optimized separately and they are fundamentally connected.

To illustrate the fundamental relationship between BV and ON-resistance of an unipolar power device, Si and GaN-based Schottky diodes (n-type) are compared in Figure 1.4. The Schottky diodes feature a drift region which is used to withstand OFF-state voltage. However, the drift region contributes to the ON-resistance as well when the diodes are forward biased. Assuming a uniform n-type doping in the lowly doped drift region, the electric field distribution in the fully depleted drift region in the off-state for Si and GaN diodes can be found in the bottom schematic of Figure 1.4. The electric field is linearly decreasing from the Schottky contact into the drift region, and the area of the indicated triangle gives the blocking voltage the diode can withstand. To

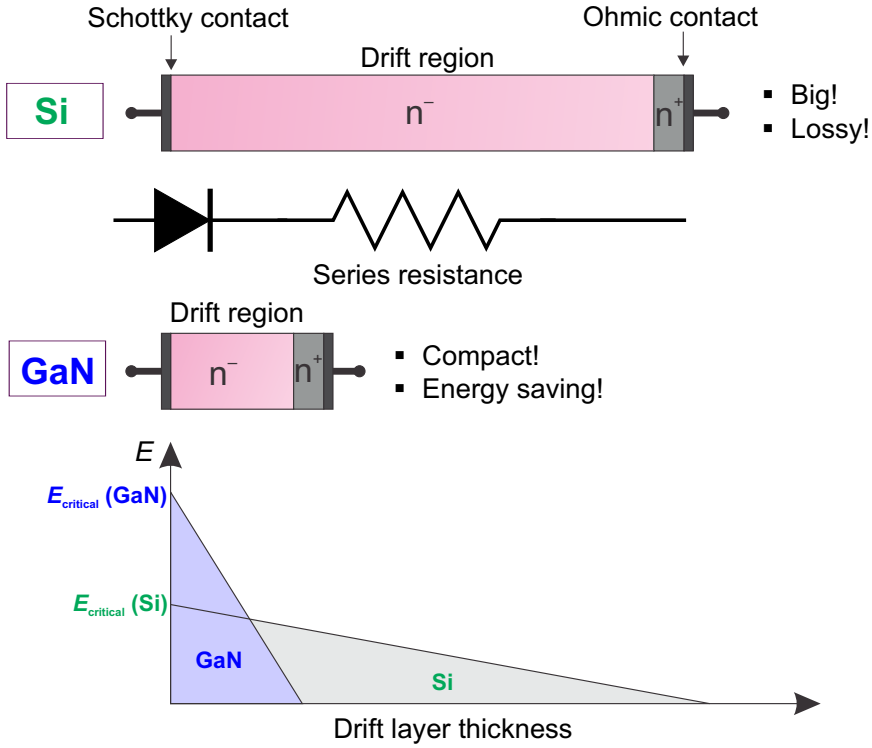


Figure 1.4: The comparison of Si and GaN Schottky diodes with the same breakdown voltage. Due to the higher critical electric field in GaN, the drift region of the GaN diode can shrink down compared with Si diode, leading to a lower poss loss in ON-state.

perform the comparison, the schematic shows the moment when the critical maximum electric field is reached at the Schottky junction and the diode starts to break down. According to Poisson's equation, the critical electric field and breakdown voltage (BV) can be described by:

$$E_{critical} = \frac{qN_D W_D}{\epsilon_0 \epsilon_r}, \tag{1.2}$$

$$BV = \frac{1}{2} E_{critical} W_D = \frac{1}{2} \frac{qN_D W_D^2}{\epsilon_0 \epsilon_r}, \tag{1.3}$$

where E_{critical}, ϵ_0, ϵ_{r}, N_{D}, and W_{D} are the critical electric field, vacuum permittivity, relative permittivity of the semiconductor, the doping concentration in the drift region, and the maximum depletion width (i.e. the entire thickness of the drift region),

respectively. In the forward operation, the ON-resistance (R_{ON}) due to the drift region can be described as:

$$R_{ON} = \rho \frac{W_D}{A} = \frac{1}{q\mu_n N_D} \frac{W_D}{A} \tag{1.4}$$

where ρ, A, μ_{n} are the resistivity, the area, and the electron mobility, respectively. Thus the specific resistance (resistance times unit area) of the ideal drift region is given by:

$$R_{ON,sp} = \frac{W_D}{q\mu_n N_D}. \tag{1.5}$$

By replacing the N_{D} and W_{D} by the expressions in equation 1.2 and 1.3, we obtain the following expression:

$$\frac{R_{ON,sp}}{BV^2} = \frac{4}{\epsilon_0 \epsilon_r \mu_n E_{critical}^3} \tag{1.6}$$

which is the so-called Baliga figure-of-merit (FOM) [2] [4]. The term ($4/\epsilon_{\mathrm{r}}\mu_{\mathrm{n}}E_{critical}^3$) is only dependent on the intrinsic properties of the semiconductor rather than the physical dimension of the device. Once the material is fixed, the ratio of $R_{\mathrm{ON,sp}}$ to BV^2 is fixed. Thus, the $R_{\mathrm{ON,sp}}$ and BV of the unipolar devices cannot be optimized independently by changing the physical dimensions. To obtain an efficient power conversion, the alternative semiconductors are needed with a lower $4/\epsilon_{\mathrm{r}}\mu_{\mathrm{n}}E_{critical}^3$ compared with the conventional silicon. It is worth mentioning that reduced surface field (RESURF) concept and Superjunction structures in silicon power devices have been proposed to improve the electric field distribution in the drift region, achieving a better trade-off between the breakdown voltage and the ON-resistance [5, 6]. However, the use of better semiconductors (i.e. SiC or GaN) can fundamentally allow for more efficient power devices compared with conventional silicon power devices.

In Figure 1.4, it shows that a GaN diode can have smaller physical size compared with a conventional silicon diode while obtaining the same breakdown voltage (the area of the triangle in the graph of the electric field profile). It is attributed to the high E_{critical} for GaN compared with Si, more details will be discussed in the following section.

1.1.2 WBG Semiconductors for Power Applications

In [7], Hudgins *et al.* presented an approximate relationship of the BV of a semiconductor with its band gap energy given by:

$$E_{critical} = 1.75 \times 10^5 (E_g)^{2.36}, \tag{1.7}$$

[2] The derivation of equation 1.6 is based on the crude assumption that BV is due to the critical field. When the field-dependent impact ionization is taken into account, the $R_{\mathrm{ON,\,sp}}$ is proportional to $\mathrm{BV}^{2.5}$ instead of $\mathrm{BV}^{2.0}$ [3].

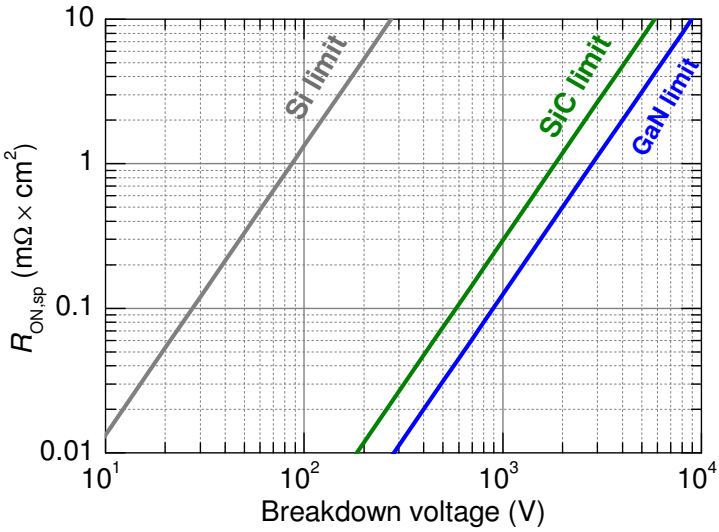


Figure 1.5: On-resistance versus breakdown voltage for Si, SiC, and GaN [8].

where E_g is the energy band gap for the semiconductor. Based on the equation 1.6, a high E_{critical} is beneficial to have efficient power devices. In Figure 1.5, the fundamental limit graph ($R_{\text{ON,sp}}$ versus BV) for Si, SiC, and GaN is shown. Due to the superior material properties, SiC and GaN as wide band gap semiconductors show promising power FOM to obtain more efficient power devices compared with conventional Si power devices.

To illustrate the idea of more efficient power conversion by using wide band gap semiconductors, we can see that 3 orders of magnitude lower $R_{\text{ON,sp}}$ for GaN devices can be achieved compared with Si devices at fixed BV. Thus less ON-state power will be dissipated in the GaN devices and a more efficient power converter can be made. Furthermore, a GaN diode can be much smaller than silicon diode based on equation 1.5, that leads to a more compact and cost-effective device.

1.2 GaN Technology for Power Electronics

This section discusses how to use GaN as a cost-effective technology for efficient power electronics.

1.2.1 Fundamental Physics of AlGaN/GaN Heterojunction

Besides the wide band gap nature of GaN-based materials, (Al)GaN with Wurtzite crystal structure shows spontaneous and piezoelectric polarization due to the lack of inversion symmetry of the crystal in the polar axis (i.e. [0001] or [000$\bar{1}$]) [9]. Figure 1.6

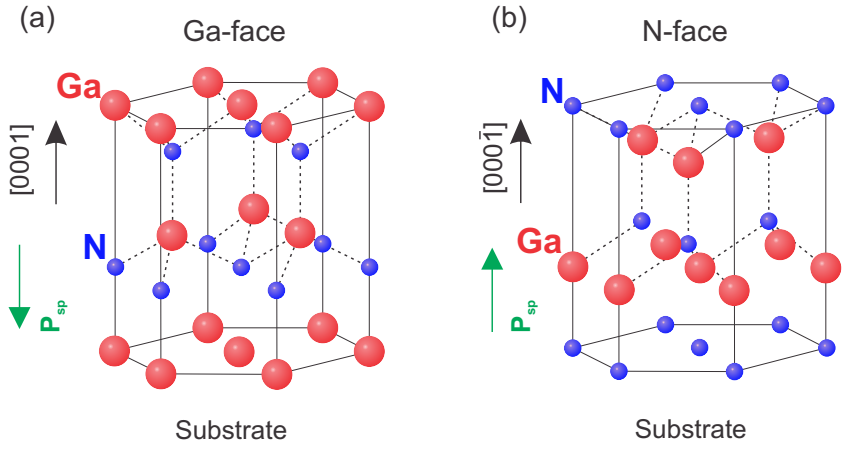


Figure 1.6: Schematic illustration of Wurtzite GaN crystal structure with Gallium-face (a) and Nitrogen-face (b) as the terminating surface [9, 11].

shows that the ideal Wurtzite GaN crystal can have Ga or N atoms as the terminating surface. It was reported that the orientation of (Al)GaN epitaxial layers grown by metalorganic chemical vapor deposition (MOCVD) is normally (0001), whereas either the (0001) or the (000$\bar{1}$) orientation can be obtained with molecular-beam epitaxy (MBE) [10]. Depending on the growth orientation, spontaneous polarization ($\boldsymbol{P}_{\mathrm{SP}}$) with different directions can exist in the epi-layers (illustrated in Figure 1.6).

The alloyed AlGaN crystal shares the same polarization properties with GaN. Additionally, AlGaN has a smaller lattice constant and a larger band gap (dependent on the Al%) compared with GaN. This gives another dimension to tune the electrical properties of GaN-based structures. Considering the AlGaN/GaN heterojunction, a conduction band offset exists at the heterointerface. Due to the lack of inversion symmetry, both AlGaN and GaN layers have spontaneous polarization in the layer as a bulk property. The AlGaN layer additionally has a piezoelectric polarization ($\boldsymbol{P}_{\mathrm{PZ}}$) as a result of the strained layer due to a smaller lattice constant compared with GaN. At the interface, a sheet of net polarization charge is present due to the divergence of the polarization field shown below:

$$\nabla \cdot \mathbf{P} = \nabla \cdot (\mathbf{P_{SP}} + \mathbf{P_{PZ}}) = -\rho_{pol}, \tag{1.8}$$

where ρ_{pol} stands for the polarization charge density (with unit of C/cm^2). In the case of a (Al)Ga-face terminated epi-stack, a net positive polarization exists at the AlGaN/GaN interface in Figure 1.7. Due to the charge compensation, a sheet of electrons is attracted at the AlGaN/GaN interface forming the so-called 2-dimensional electron gas (2DEG). Figure 1.7 shows the simulated band diagram of an AlGaN/GaN

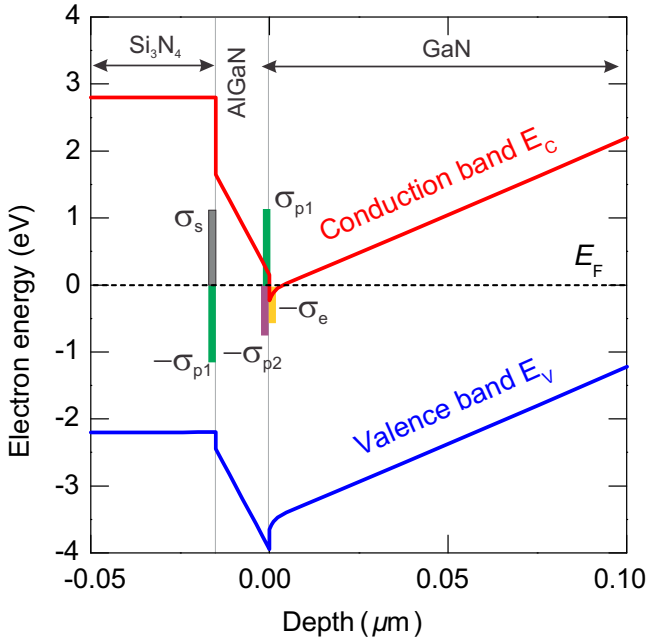


Figure 1.7: Simulated energy band diagram of AlGaN/GaN heterojunction, Si_3N_4 is used to passivate the AlGaN surface.

heterojunction. Due to the band off-set at the AlGaN/GaN interface, a quantum well is formed where the 2DEG is residing. It is believed that surface states (σ_S)at the AlGaN surface provide the source of electrons for the 2DEG channel [12]. The 2DEG can reach a sheet density as high as 10^{13} cm^{-2} and an electron mobility of $\sim$ 2000 cm^2/V $\cdot$ s. These properties of AlGaN/GaN heterojunction make it promising for high-power and high frequency applications.

1.2.2 AlGaN/GaN-on-Si Technology

The sheet density and electron mobility of the 2-dimensional electron gas at the AlGaN/GaN interface are highly dependent on the epitaxial quality. Due to the unavailability of large wafer size and high quality GaN bulk substrates (two inches or below), extensive efforts have been made to grow AlGaN/GaN structures on foreign substrates. To enable low-cost production of GaN-based devices, many research groups have been developing AlGaN/GaN epi-layers on large-area silicon substrates [13, 14]. Figure 1.8 presents an example of (Al)GaN layers on silicon substrate. It starts with an AlN nucleation layer. Due to the large lattice mismatch and thermal coefficient mismatch between GaN and silicon, step-graded AlGaN buffer layers were used to gradually reduce the crystal defects from bottom to the top. Finally, high-

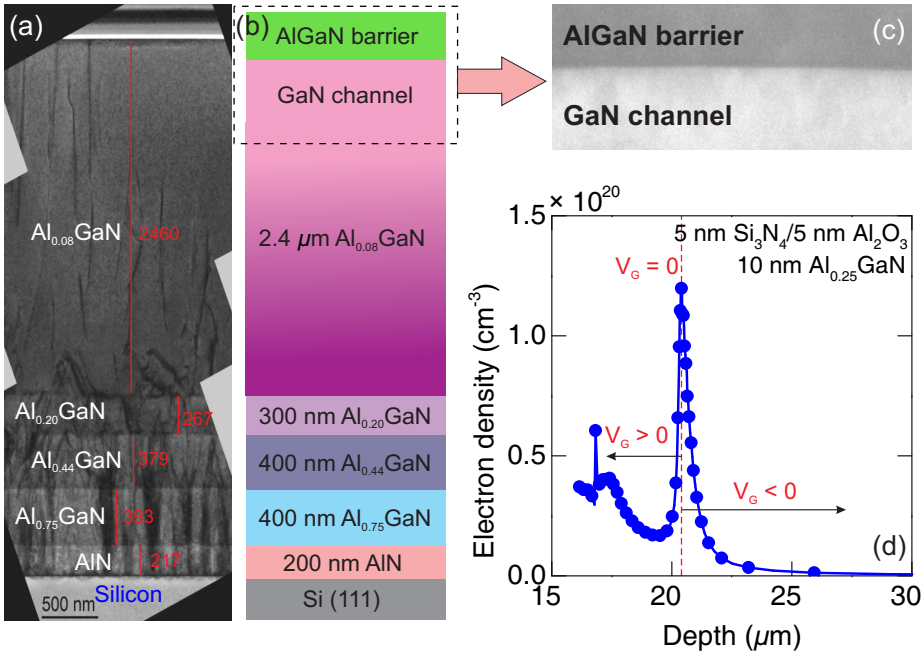


Figure 1.8: (a) and (b) The cross-sectional TEM image of the epi-stack on a 200-mm silicon substrate. (c) The TEM image of the AlGaN barrier and GaN channel. (d) The 2DEG depth profile in an AlGaN/GaN structure. *Courtesy: Dr. M. Zhao and Dr. M. Van Hove, imec.*

quality crystalline AlGaN barrier and GaN channel layers were obtained (shown in Figure 1.8(c)). From the capacitance–voltage profile in Figure 1.8(d), we confirm the presence of high 2DEG sheet density at the AlGaN/GaN heterointerface [9]. Lateral AlGaN/GaN high electron mobility transistors (HEMTs) and Schottky barrier diodes (SBDs) can be made by utilizing the superior properties of the 2DEG. The devices studied in this PhD project were fabricated on state-of-the-art 200-mm GaN-on-Si wafers fabricated in the imec processing line [15].

1.2.3 Au-free CMOS Compatible Technology

In the previous section, the fundamental physics related to the formation of the 2DEG at the wide band gap un-doped AlGaN/GaN heterojunction was described. However, it is challenging to make an ohmic contact to the 2DEG due to the highly resistive AlGaN barrier layer on top of the quantum well. In literature, typical ohmic metallization schemes consist of the deposition of a Au-based metal stack directly on the AlGaN barrier, followed by a rapid thermal annealing (RTA) step at high temperature [16, 17].

To enable the integration of GaN-based electronic devices in existing Si CMOS process

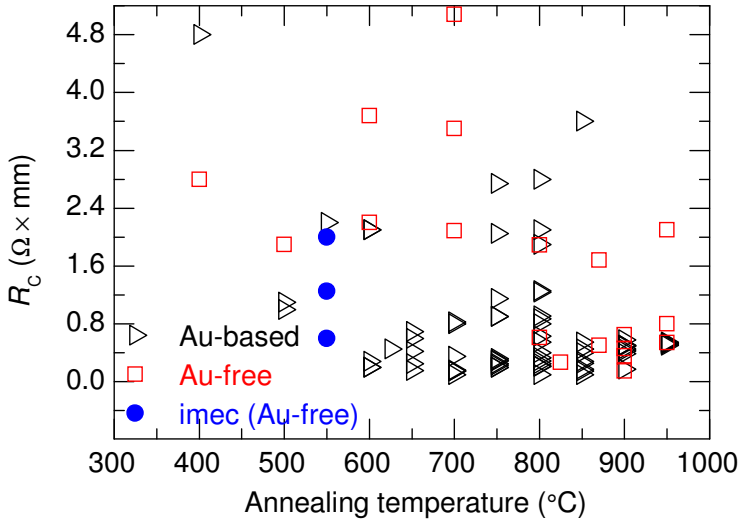


Figure 1.9: Contact resistance versus annealing temperature for Au-based, Au-free, Ti/Al-based ohmic contacts developed at imec [17].

lines and substantially reduce the production cost for large volume fabrication, Au-free metallization schemes are required because of the contamination issues of using Au/Pt-based metals. Moreover, it is important to lower the thermal budget from the integration purpose point of view. At imec, Au-free low temperature ohmic contacts have been developed [17]. Firrincieli *et al.* studied the impact of RTA temperature and Ti/Al ratios on the ohmic contact resistance and presented a low contact resistance of ~ 0.62 $\Omega \cdot$ mm with a thermal budget at 550 °C [17]. In Figure 1.9, the benchmarking graph of contact resistance versus annealing temperature for Au-contained, and Au-free ohmic contacts is shown. By optimizing the Ti/Al ratio, the challenge of obtaining sub-1.0 $\Omega \cdot$ mm contact resistance for Au-free ohmic contacts has been tackled [15, 17, 18].

1.3 Objectives of the Dissertation

Due to the high sheet electron density and high electron mobility of the 2DEG at the wide band gap AlGaN/GaN heterointerface, efficient power transistors and diodes can be fabricated. The low-cost production of the GaN-based devices on imec 200-mm GaN-on-Si wafers with CMOS-compatible process flows can enable a breakthrough of GaN technology in the power conversion market.

Figure 1.10 presents the cross-section of an AlGaN/GaN diode and an AlGaN/GaN transistor (i.e. AlGaN/GaN MISHEMT as an example) based on the GaN-on-silicon technology. Due to the nature of "surface conduction" in lateral devices, GaN-on-Si technology offers the feasibility to monolithically integrate the GaN HEMT

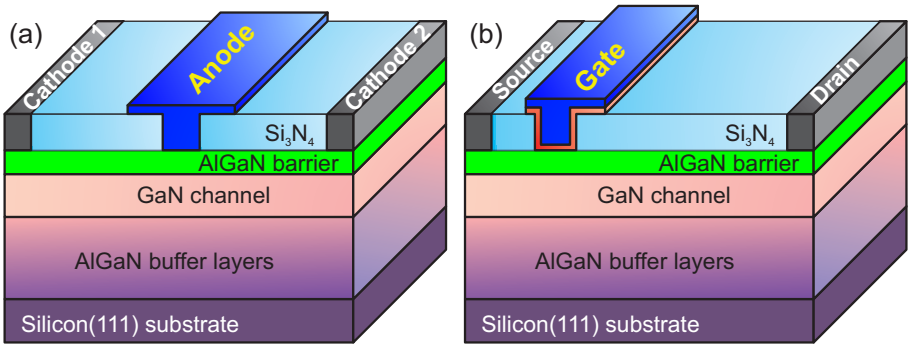


Figure 1.10: The schematics of AlGaN/GaN SBD (a) and HEMT (b) on silicon substrate.

and SBD together on the substrate. Discrete GaN HEMT and SBD based on the AlGaN/GaN structure are promising as well for high-power switching applications. When this PhD project started, many research groups have been working on GaN transistors for radio-frequency [19], high-power [20], switching applications [16], etc. Approaches like recessed-gate [21], p-GaN gate [22,23], F-implantation [24], etc. have been proposed to obtain enhancement-mode GaN transistors. Furthermore, reliability issues in GaN transistors have been widely studied in literature [25–27]. At imec, we have been working on both the GaN diode and transistor fabricated on 200-mm silicon wafers with a Au-free CMOS compatible process for high-power switching applications. Thanks to Dr. M. Zhao as the Epi-engineer, Dr. S. Lenci and ir. B. De Jaeger as the process integration engineers at imec, this PhD project focuses on the electrical characterization and simulations of GaN diodes to understand the underlying operational principles, improve the DC and dynamic characteristics, and investigate initial reliability mechanisms.

Figure 1.11 shows the typical leakage and on-state characteristics of a Au-free AlGaN/GaN Schottky barrier diode for both floating and grounding substrate configurations. It shows a high leakage current of 1 mA/mm and a lower device BV (∼400 V) when the substrate is grounded. On-state characteristics are independent of the substrate connection due to the relatively low voltage bias at the surface. To obtain low leakage and low onset voltages for GaN diodes remains to be a challenge which needs to be tackled in this thesis. The dynamic characteristics involving electron trapping/de-trapping kinetics for GaN diodes are unclear. The reliability issues under high current and high voltage stress for AlGaN/GaN diodes have not been explored yet. The scope of this research work covers the following two main parts.

The first part of the thesis is dedicated to the leakage reduction and on-state improvement of the AlGaN/GaN by designing embedded edge termination, using carbon-doped buffers to enhance the buffer BV, optimizing anode metallization schemes, and applying anode recess process, etc. The performance and figure-of-merit ($BV^2/R_{ON,sp}$)

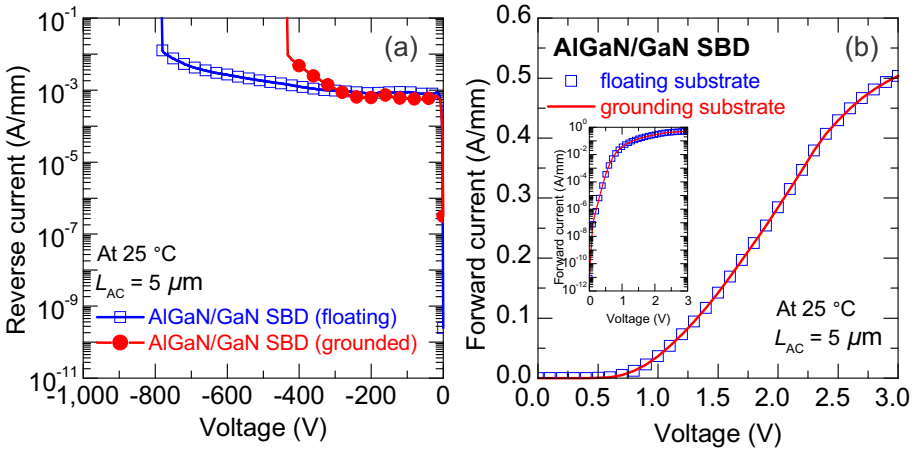


Figure 1.11: (a) Leakage characteristics of AlGaN/GaN SBD in floating and grounded substrate configurations. (b) Forward characteristics of AlGaN/GaN SBD in floating and grounded substrate configurations.

of our optimized Au-free GaN diodes needs to be benchmarked with the data from literature.

A second goal of this thesis is to investigate the root causes impacting the dynamic stability of the GaN diodes and implementing techniques to improve it. Initial reliability issues are investigated as well. TCAD simulations are used to understand the field-assisted trapping and degradation mechanisms.

1.4 Outline of the Thesis

In chapter 2, the DC characteristics of integrated AlGaN/GaN Schottky barrier diodes are investigated experimentally. It is demonstrated that by implementing the design of an embedded edge termination in the anode trench and anode recess process, the leakage and forward characteristics of AlGaN/GaN SBDs can be improved simultaneously.

In chapter 3, further performance optimization is described for the AlGaN/GaN SBDs with gated edge termination. A carbon-doped AlGaN buffer is selected due to its lower buffer leakage and higher buffer breakdown voltage than those of UID buffer. With this carbon-doped buffer, the AlGaN/GaN GET-SBDs show promising reverse characteristics for 200 V applications. A further leakage reduction is demonstrated by optimizing the TiN anode metallization scheme without degrading the on-state characteristics. By benchmarking, the optimized AlGaN/GaN SBDs show the best performance in terms of low leakage and low forward voltage realized in Au-free technology. Moreover, the evaluation of the large power diodes on 200-mm silicon

substrate demonstrates excellent characteristics with good yield and uniformity (at both 25 °C and 150 °C).

In chapter 4, the motivation and measurement procedures to assess the dynamic characteristics of GaN diodes are discussed. Pulsed current–voltage and current-based transient measurements are developed to evaluate the trapping/de-trapping mechanisms when the diode is subject to off-state stress. Dominant surface trapping is observed, and an improvement is experimentally realized by using cleaning steps and a better passivation layer and dielectrics.

In chapter 5, an extensive trapping analysis is performed on GaN diodes fabricated on intentionally carbon-doped buffer layers. The carbon-doped (Al)GaN buffer can effectively suppress the buffer parasitic leakage current, however, it can potentially degrade the stability properties of the GaN diodes. To identify the buffer trapping mechanism, current transient measurements on SBD and TLM structures are performed. TCAD simulation is also used to analyze the trapping effects in AlGaN/GaN diodes with edge termination. Finally, a significant improvement of the stability in GaN diodes is shown to be achieved by using a low-trapping [3] buffer for the fabrication of GaN diodes.

In chapter 6, ON- and OFF-state accelerated stress tests are reported to evaluate the long term stability and reliability characteristics of high performance GET-SBD devices. The degradation modes under different stress conditions in both ON- and OFF-state are experimentally investigated. Based on the voltage-acceleration tests, the device lifetime can be evaluated targeting at specified voltage applications. The GET-SBD demonstrates good device reliability under ON-state stress. Time-dependent breakdown mechanism in GET-SBD, under OFF-state stress, can lead to permanent leakage degradation and eventually the device failure limiting its high-voltage applications.

Finally, chapter 7 presents the conclusions and future work on this subject.

[3] In literature, the term “dispersion” was frequently used to describe the dynamic R_{ON} phenomenon of GaN-based devices. However, “dispersion” typically relates to a frequency-dependent phenomenon (i.e. phase velocity of a wave in optics, capacitance-voltage (C-V) characteristics of MOS structure, etc.). In this thesis, we choose to use the terminology “low-trapping” or “trapping-free” instead of “dispersion-free”, dynamic R_{ON} increase instead of R_{ON} dispersion.

Chapter 2

AlGaN/GaN Diodes: Leakage Reduction and On-State Improvement

In this chapter, the DC characteristics of integrated AlGaN/GaN Schottky barrier diodes are investigated experimentally, tackling the challenge of achieving low leakage current and low forward voltage for high-performance power diodes.

2.1 Introduction

Schottky barrier diodes based on AlGaN/GaN heterojunction are promising for power switching applications. One important aspect is that SBDs are unipolar devices with fast switching capability and low reverse recovery current during turn-off [28]. However, one fundamental challenge towards the integration of AlGaN/GaN Schottky barrier diodes (SBDs) with existing high-performance AlGaN/GaN high electron mobility transistors (HEMTs) is to fabricate a high performance diode with low leakage and low forward voltage, so that efficient power systems based on GaN technology can be achieved [29]. In chapter 1, we saw that the leakage current for conventional AlGaN/GaN SBD is high. This leads to static power loss and potential reliability issues. Consequently, a systematic investigation of the reverse and forward characteristics of AlGaN/GaN Schottky barrier diodes is required.

To reduce leakage, existing studies were focused on the design of field plates and device architectures [30], the selection of the anode metal [31,32], and various cleaning process steps [33, 34]. High leakage current was observed in conventional [1] Au-free AlGaN/GaN SBDs due to the presence of a high electric field at the perimeter of the Schottky contact in the off-state [35]. Due to this reason, in this chapter two device architectures with different edge termination [2] approaches are investigated to suppress the peak electric field, thus achieving a low leakage current.

Regarding the on-state operation, the electrons in the 2DEG need to flow through the high-resistive AlGaN barrier layer. The Schottky barrier height (∼1 eV) and thick layer of AlGaN barrier layer in a conventional AlGaN/GaN SBD render it difficult

[1] A conventional AlGaN/GaN diode has the simplest diode structure without dedicated design of edge terminations. It will be used as the reference device compared with other diode architectures where we design edge termination structure to shape the electric field distribution.

[2] Edge termination is a special termination structure used to shape the electric field distribution around the edges of the power devices [2].

for electrons to overcome or tunnel through the energy barrier, resulting in high ON-state voltages for the diode. The AlGaN barrier recess process allows for higher tunneling currents in the on-state by shortening the tunneling distance. Combining the process of barrier recess with the design of device architectures, the feasibility of achieving AlGaN/GaN SBD with low leakage current and low forward voltage drop is demonstrated.

It will be also shown that the buffer leakage and breakdown dominate the diode off-state characteristics when the reverse voltage exceeds 300 V. A more resistive buffer is needed to allow for high voltage AlGaN/GaN SBD with strong off-state blocking capability.

2.2 Leakage Mechanism in Conventional AlGaN/GaN SBDs

The goal of this section is to understand the features of the leakage current in conventional AlGaN/GaN SBDs fabricated with Au-free CMOS technology. The dependence of leakage current on temperature and layout parameters has been studied, showing that the high leakage current in the conventional AlGaN/GaN SBD is dominated by tunneling current at its perimeters. This hypothesis has been further verified by the TCAD simulations which show an enhancement of the electric field at the anode edge.

2.2.1 Experimental Details

AlGaN/GaN heterostructure epitaxial layers have been grown on 200-mm diameter silicon wafers by metalorganic chemical vapor deposition (MOCVD). The epi-stack consists of 15 nm $Al_{0.21}Ga_{0.79}N$ barrier, a 150 nm GaN channel layer, a unintentionally doped (UID) buffer layer (400 nm $Al_{0.74}Ga_{0.26}N$/400 nm $Al_{0.44}Ga_{0.66}N$/1800 nm $Al_{0.21}Ga_{0.79}N$), and a 200 nm AlN nucleation layer on p-type Si <111> substrates. The wafers are capped with ~2 nm AlGaN layer, and a passivation layer of 140 nm Si_3N_4 has been deposited on the whole epitaxial stack by means of rapid thermal chemical vapor deposition (RTCVD) at 750 °C.

To form the anode and cathode contacts, an "Anode-first" approach has been used which is compatible with existing CMOS process flows. The removal of the Si_3N_4 passivation layer in the anode region is performed by SF_6 dry etching. The Au-free anode metal stack is composed of 20 nm TiN/20 nm Ti/250 nm Al/20 nm Ti/60 nm TiN deposited by physical vapor deposition at 25 °C. Prior to the deposition of the cathode metal stack, a dry etching process of the RTCVD capping nitride and the AlGaN barrier layer in the contact area is performed [17]. The ohmic contacts are formed with a stack of 20 nm Ti/200 nm Al/20 nm Ti/60 nm TiN which are annealed at 550 °C. A schematic structure of the conventional AlGaN/GaN SBD is shown in Figure 2.1 (a). Scanning electron microscope (SEM) images of the anode and cathode region of fabricated AlGaN/GaN SBDs are presented in Figure 2.1 (b) and (c), respectively. There is a 1-μm anode metal overhang on the 140-nm Si_3N_4 passivation layer toward the cathode contact acting as a field plate (F.P.). The Schottky contact length L_{SC} and the anode-to-cathode spacing L_{AC} in the tested SBDs are 9 μm and 10 μm, respectively.

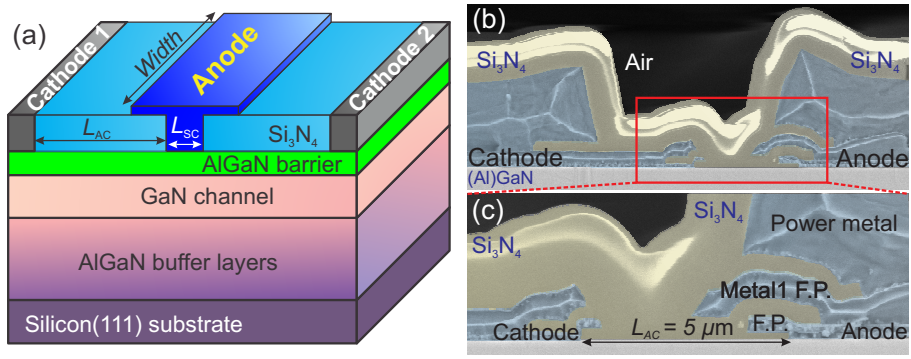


Figure 2.1: (a) Cross-sectional schematic of a conventional AlGaN/GaN Schottky barrier diode fabricated on a silicon substrate, the back-end structure is not shown here. (b) The scanning electron microscope (SEM) image of the AlGaN/GaN SBD showing the anode and cathode contacts. (c) A zoomed-in SEM image of the AlGaN/GaN SBD showing the field plates (F.P.) and the anode-to-cathode spacing L_{AC}.

2.2.2 Leakage Characteristics

The conventional AlGaN/GaN SBD leakage characterizations have been performed (on-wafer measurements) on single-finger small diodes (100 μm width) by using a Semiconductor Device Analyzer (Agilent B1500A) at different temperatures.

Typical temperature-dependent off-state characteristics of conventional AlGaN/GaN SBDs down to a reverse voltage (V_R) of −100 V are displayed in Figure 2.2(a). With the increase of reverse voltage from 0 to −100 V, there is a vertical depletion of the 2DEG at the AlGaN/GaN interface followed by a lateral depletion in the access region. The extended depletion region withstands the majority of the reverse voltage instead of the thin AlGaN barrier layer [36].

From the results shown in Figure 2.2(a), the conventional AlGaN/GaN SBD shows a high leakage current of 1 mA/mm (leakage normalized to the width of the anode finger) which starts already at $\sim$ −10 V (after the vertical depletion of 2DEG). The off-state characteristics show a weak temperature-dependence in the box-and-whisker plot of Figure 2.2(a). A Whisker plot (data from 26 diodes) of the diode leakage current at V_R of −100 V at different temperatures (from 273 to 473 K) is shown in Figure 2.2(b). It confirms the weak temperature sensitivity of the leakage, and the leakage only shows a 2-fold increase from room temperature (273 K) measurement to the one at 200 °C (473 K). This indicates a dominant contribution of tunneling current in the leakage current of AlGaN/GaN conventional SBDs, since the tunneling component is known to be weakly temperature dependent.

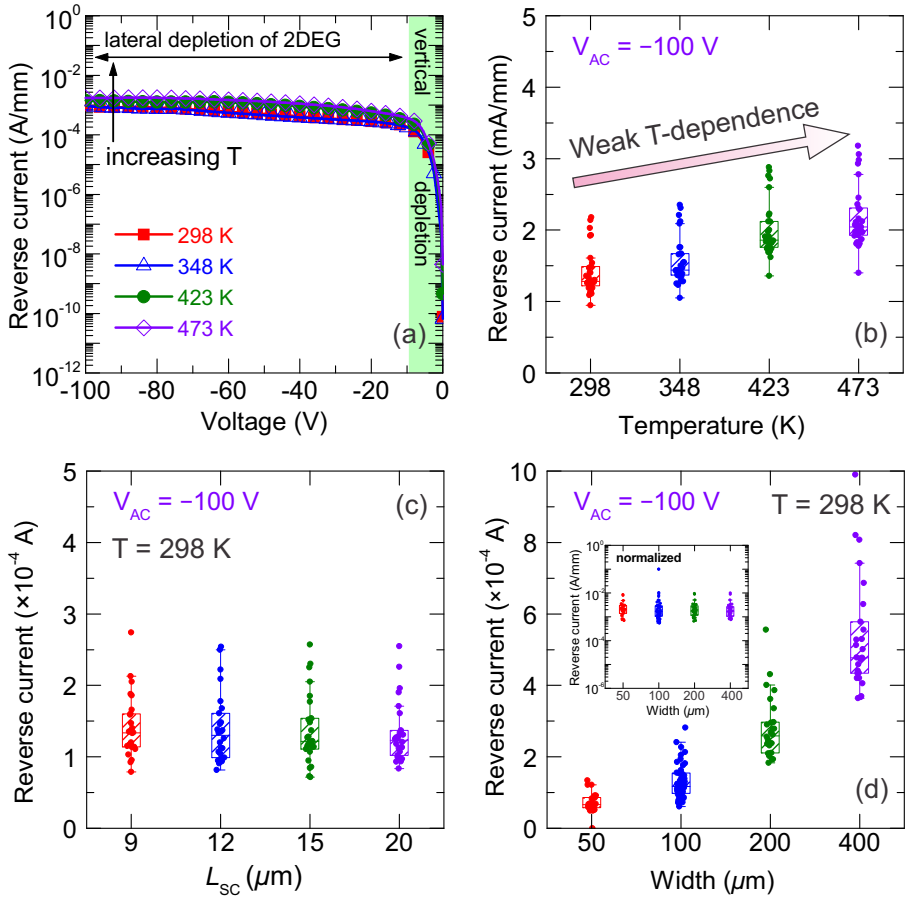


Figure 2.2: (a) The leakage current of the conventional AlGaN/GaN SBD measured at different temperatures. (b) Statistical data (26 devices) of the leakage current at V_R of −100 V for different temperatures. (c) Statistical plot of the leakage current at V_R of −100 V for SBDs with different Schottky contact length L_{SC}. (d) Statistical results of the leakage current at V_R of −100 V for SBDs with different anode finger width.

The dependence of leakage current on the area of the Schottky contact is studied by varying the Schottky contact length and width of the anode finger width independently. As is shown in Figure 2.2(c) and (d), the leakage current (at V_R of −100 V) is invariant with the change of Schottky contact length L_{SC}, but shows a linear dependence on the width of the anode finger. The inset graph of Figure 2.2(d) shows the normalized leakage current to the width of the anode finger. After the normalization, the leakage current is invariant taking the statistical distribution into account. With the results shown in Figure 2.2, we are able to conclude that the leakage of the conventional AlGaN/GaN SBDs features a perimeter-scaling dependence. The leakage current is dominated by tunneling component which should correlate with the peak electric field at the corner of the Schottky contact. In the next section, TCAD electrical simulations will be performed to visualize the electric field distribution in the diode off-state operation and support the hypothesis.

2.2.3 TCAD verification

2.2.3.1 Interface State Model and 2DEG Density Calibration

Two-dimensional TCAD simulations of AlGaN/GaN heterostructures have been carried out by using the commercial software Synopsys Sentaurus Device, wherein the Poisson and the continuity equation are solved self-consistently [37]. The DC and dynamic characteristics of GaN diodes and HEMTs are reported to be strongly affected by the surface donor-like states which are commonly known as a major source of the electrons for the formation of the two-dimensional electron gas (2DEG) channel at the AlGaN/GaN interface [12, 38–40]. The surface-donor model has been defined in the simulation structure at the interface between the AlGaN barrier and the Si_3N_4 passivation layer, the interface states are defined at a discrete energy level of 1.65 eV with a density equal to the surface dipole charge density for compensation [41]. This energy level was also reported in the paper by Ibbetson *et al.* and used to pin the Fermi level at the AlGaN surface [12]. Due to both spontaneous and piezoelectric polarizations in the strained AlGaN barrier layer (with Ga-face), negatively charged bound charges are present at the AlGaN surface [9,40,42]. The donor-states are ionized with positive charges compensating the bound polarization charges, resulting in the formation of a 2DEG at the quantum well at the AlGaN/GaN interface [41].

In samples with an Al mole fraction of 35% in the AlGaN barrier, the polarization charge density ($-\sigma_{p1}$) at the AlGaN surface is calculated to be 3.70×10^{13} cm^{-2}, and the net polarization charge density ($\sigma_{p1} - \sigma_{p2}$) at the $Al_{0.35}Ga_{0.65}N$/GaN interface is 1.89×10^{13} cm^{-2}. The net positively charged dipoles attract electrons to the interface and form the 2DEG channel due to the charge neutrality condition [12]. In Figure 2.3(a), a high electron density is shown at the AlGaN/GaN interface from the simulated AlGaN/GaN Schottky diode structure. By taking a vertical cut-line at the place between the Schottky contact and the cathode contact (i.e. the access region), the simulated band diagram at equilibrium state can be plotted and is shown in Figure 2.3(b). The Fermi-level E_f is uniform through the whole system, and is shown to be located above the conduction band at the quantum well at the AlGaN/GaN heterointerface resulting in the high-density 2DEG with a high electron mobility

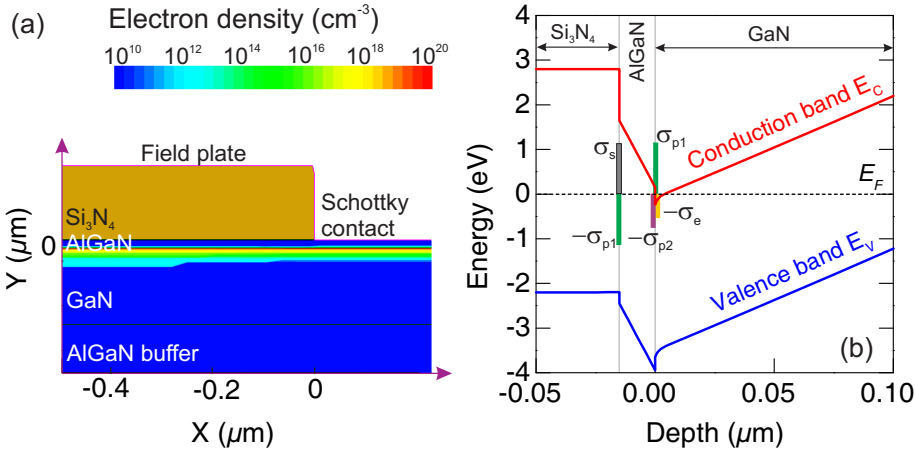


Figure 2.3: (a) Two-dimensional visualization of the electron density at equilibrium in the simulated Schottky diode structure. (b) The simulated band diagram (at equilibrium) obtained by taking a cut-line between the Schottky contact and the cathode contact (the so-called access region).

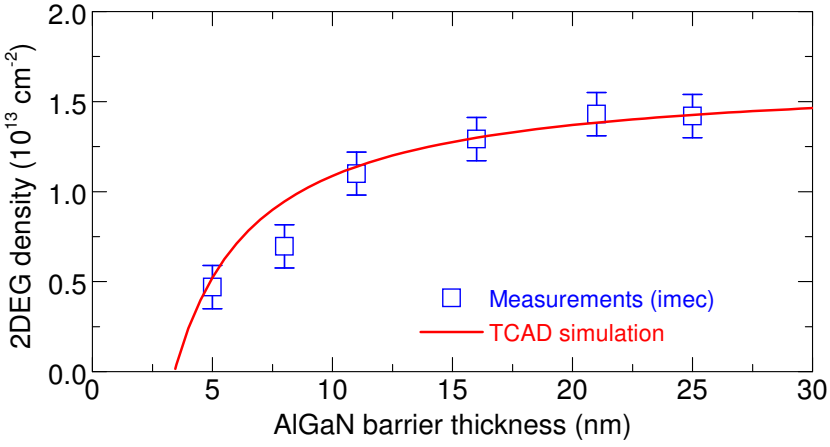


Figure 2.4: 2DEG density at the $Al_{0.35}Ga_{0.65}N$/GaN interface as a function of the AlGaN barrier thickness with the comparison of experimental data and TCAD simulations [41].

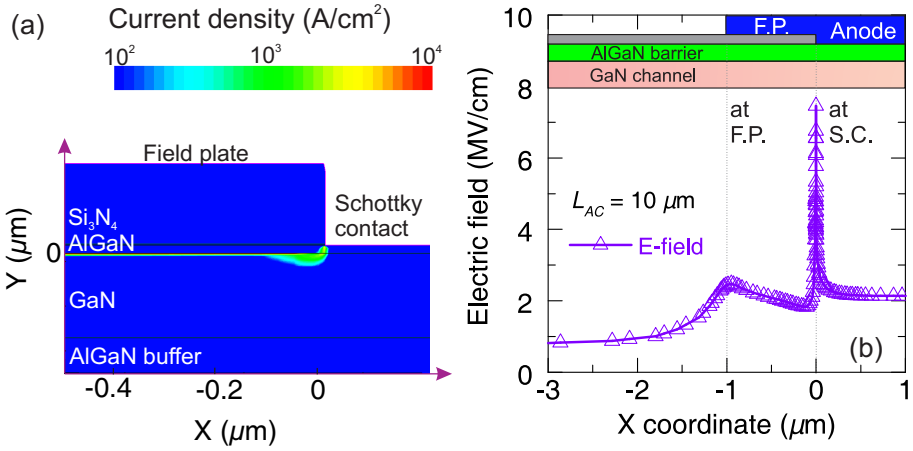


Figure 2.5: (a) The simulated current density for the AlGaN/GaN SBD at V_R of −100 V. (b) The lateral electric field distribution in the AlGaN barrier at V_R of −100 V.

[43]. The linear band bending in AlGaN and GaN layers is due to the incomplete compensation of charges at the interfaces, consequently a constant electric field is present in the layer.

Since the 2DEG is one of the most important features of the AlGaN/GaN heterojunction, the 2DEG density as a function of the $Al_{0.35}Ga_{0.65}N$ barrier layer has been studied in experiments and simulations [41]. Figure 2.4 shows that the 2DEG density increases with the AlGaN barrier thickness and starts to saturate when the thickness is larger than ∼12 nm. With the model defined in TCAD, the simulation results show a very good overlay with the experimental data. The calibrated TCAD will be used for the electrical simulations on AlGaN/GaN diodes.

2.2.3.2 Off-State Simulation

To validate the perimeter-scaling effect of the leakage current in conventional AlGaN/GaN SBDs, an off-state TCAD simulation on the diode structure is performed with the simulator settings as previously defined in section 2.2.3.1. In the simulator, a nonlocal tunneling model [37] has been used and defined at the anode contact. In Figure 2.5(a), the simulated leakage current density at V_R of −100 V for the conventional diodes is shown. It can be clearly seen in Figure 2.5(a) that the leakage current path is located at the edge of the Schottky contact. The electric field distribution at V_R of −100 V inside the AlGaN barrier is plotted in Figure 2.5(b) by taking a lateral cut-line in the barrier layer (0.5 nm away from the AlGaN/Si_3N_4 interface). A peak electric field is observed at the anode edge, a second peak is due to the capacitive coupling from the field plate overhang on the 140-nm Si_3N_4 layer. The peak electric field at the anode edge results in a severe band bending. As a consequence, the electrons

from the anode contact can tunnel through the AlGaN barrier layer resulting in a high leakage current, which has been experimentally shown in section 2.2.2.

With the simulation results in Figure 2.5, the leakage characteristics can be explained by the tunneling mechanism which is known to be weakly temperature dependent [44]. The high leakage current in conventional AlGaN/GaN SBDs results from the enhancement of the electric field at the anode edge. To obtain a low leakage current in the diodes, a technique to suppress the peak electric field at the corner of the Schottky contact becomes mandatory.

2.3 Integrated GaN Diodes with Edge Termination

To reduce the leakage current in AlGaN/GaN diodes, two device architectures with edge terminations are studied to suppress the peak electric field at the anode edge: AlGaN/GaN SBD with gated edge termination (GET-SBD) and AlGaN/GaN SBD with external edge termination (EET-SBD).

2.3.1 Process Flow for Integrated GaN Diodes

The goal of this section is to show the process flows for the integration of GaN diodes with GaN MISHEMTs. Architectures with edge terminations have been designed to suppress the peak electric field at the perimeter of the Schottky contact. Detailed process steps for the integration of edge terminated GaN diodes with MISHEMTs will be shown. The Si_3N_4, which has been used as the gate insulator in MISHEMTs, will be used as the material for the edge termination in AlGaN/GaN SBDs [15].

In Figure 2.6(a) and (b), the process flows for the fabrication of AlGaN/GaN SBDs with two types of edge terminations (gate edge termination and external edge termination) are shown. The AlGaN/GaN layers grown on a silicon substrate are used for the fabrication of both AlGaN/GaN MISHEMTS and SBDs. Prior to the processing, the AlGaN surface is protected by a 140-nm Si_3N_4 layer deposited by rapid thermal chemical vapor deposition (RTCVD) at 750 °C. The nitrogen implantation technique is used for the interdevice isolation. When the RTCVD Si_3N_4 is opened, the exposed AlGaN barrier can be recessed by atomic layer etching (in the case of recessed SBDs) which is an approach used for recessed gate enhancement-mode GaN HEMTs [21]. When the SBDs are recessed, the remaining AlGaN barrier thickness is $\approx$ 5 nm (in this chapter). In contrast with the device process of conventional AlGaN/GaN SBD described in section 2.2.1, a thin ($\sim$15 nm) Si_3N_4 is deposited by rapid thermal chemical vapor deposition (RTCVD) as the material for the edge termination in the anode trench. This Si_3N_4 can act as the gate dielectric for the AlGaN/GaN MISHEMTs on the same wafer [29]. The central region of the Si_3N_4 can be etched away prior to the deposition of anode metals. A TiN-based stack is deposited and patterned to define the anode region. The Au-free ohmic contacts are fabricated with a Ti/Al-based stack and annealed at 550 °C. The back-end consists of 4-μm thick Al power metallization and plasma enhanced chemical vapor deposited (PECVD) Si_3N_4 as the intermetal dielectric (not shown in Figure2.6) [29]. As can be seen in Figure 2.6(a) and (b), the GET-SBD has a more compact structure by embedding the edge termination inside the anode

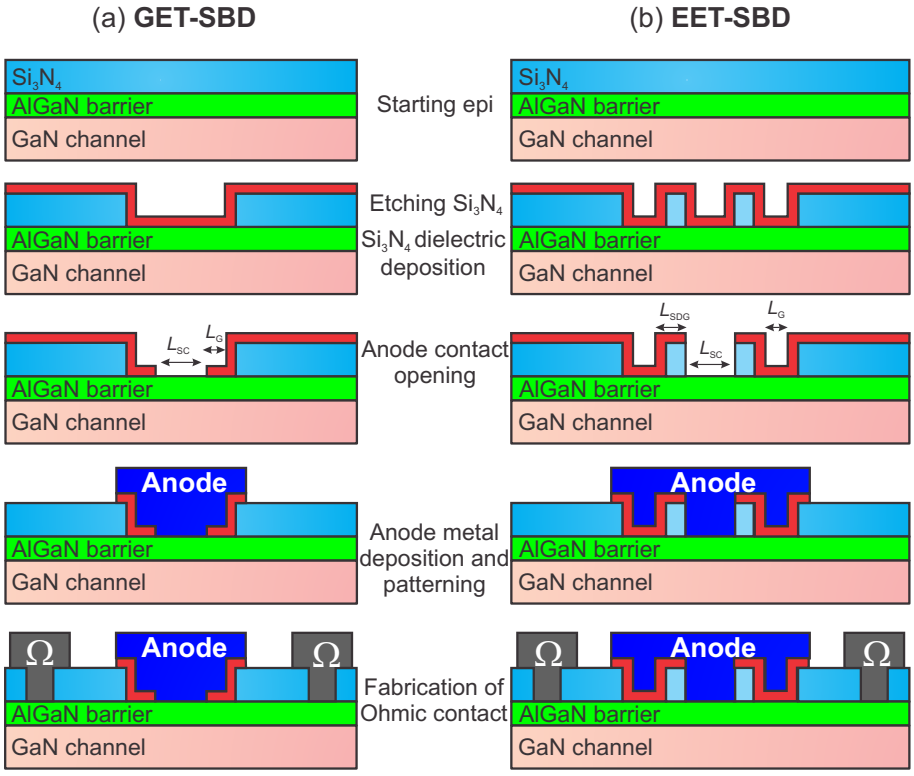


Figure 2.6: (a) The process steps for the fabrication of an AlGaN/GaN SBD with gated edge termination (GET-SBD) and (b) an AlGaN/GaN SBD with external edge termination (EET-SBD). The starting epi-structure is the AlGaN/GaN heterojunction whose surface is encapsulated by a 140-nm Si_3N_4.

trench comparing with the EET-SBD architecture due to the feature of an external edge termination in EET-SBD. The spacing between the Schottky contact and the external edge termination is named as L_{SDG} as shown in Figure 2.6(b).

2.3.2 Electrical Results and Discussion

On-wafer off-state characterization has been performed on conventional AlGaN/GaN SBDs, GET-SBDs, and EET-SBDs by grounding the cathode and biasing the anode from 0 to −100 V using an Agilent 4073 Ultra Advanced Parametric Tester. The substrate contact is kept floating for these measurements to firstly explore the leakage current of the intrinsic diodes. All the tested diodes have an anode finger width = 100 μm and 1-μm anode metal overlapping toward the cathode. The Schottky contact length (L_{SC}) is 6 μm, and 5 μm for GET-SBD and EET-SBD, respectively. The standard length of the edge termination (L_G) is 1.5 μm for GET-SBD and EET-SBD. The leakage current is normalized to the anode finger width.

The reverse characteristics of the reference SBD, EET-SBD, and GET-SBD (with anode-to-cathode spacing of 10 μm) for non-recessed and recessed wafers are shown on Figure 2.7(a) and (c). With the increase of the reverse voltage, the leakage current shows different voltage-dependence (the slope of the leakage with respect to the voltage). This is ultimately attributed to how the 2DEG is depleted in the architecture and eventually how the electric field is distributed in the off-state. Non-recessed EET-SBD shows slightly lower leakage current than conventional SBD, while non-recessed GET-SBD demonstrates four orders of magnitude reduction in leakage. To understand the difference between the EET-SBD and GET-SBD, a statistical plot (26 devices) of the leakage current at V_R of −100 V for conventional SBDs, non-recessed GET-SBDs, and non-recessed EET-SBDs with different L_{SDG} is shown in Figure 2.7(b). Recessed EET-SBDs in Figure 2.7(c), due to a lower 2DEG density and stronger capacitive coupling to the 2DEG channel, show two orders of magnitude reduction as compared with the reference SBDs. The recessed GET-SBD with embedded edge termination in the anode trench still features the lowest leakage current.

Figure 2.7(d) presents the statistical leakage value at V_R of −100 V for conventional SBDs, recessed GET-SBDs, and recessed EET-SBDs with different L_{SDG}. The median leakage value for recessed GET-SBD at V_R of −100 V is $\sim 10^{-7}$ A/mm. From the results presented in Figure 2.7(b) and (d), it is observed that the spacing (L_{SDG}) between the edge termination and the Schottky contact plays an important role in determining the leakage current. The GET-SBD with an embedded edge termination can be thought of having an L_{SDG} of 0 μm in a EET-SBD, and the GET-SBD experimentally shows a significant reduction of the leakage current. As shown in Figure 2.7(b) and (d), the leakage current in the EET-SBD only shows a slight reduction by scaling down the dimension L_{SDG} from 4 to 0.25 μm. However, a significant drop in leakage can be achieved by embedding the edge termination inside the anode trench as in the GET-SBD architecture. This trend has been observed for both non-recessed and recessed wafers. The recessed GET-SBD architecture, though with a thinner AlGaN barrier layer, does not show degradation of the leakage current at V_R of −100 V compared with non-recessed GET-SBD. This indicates that the leakage

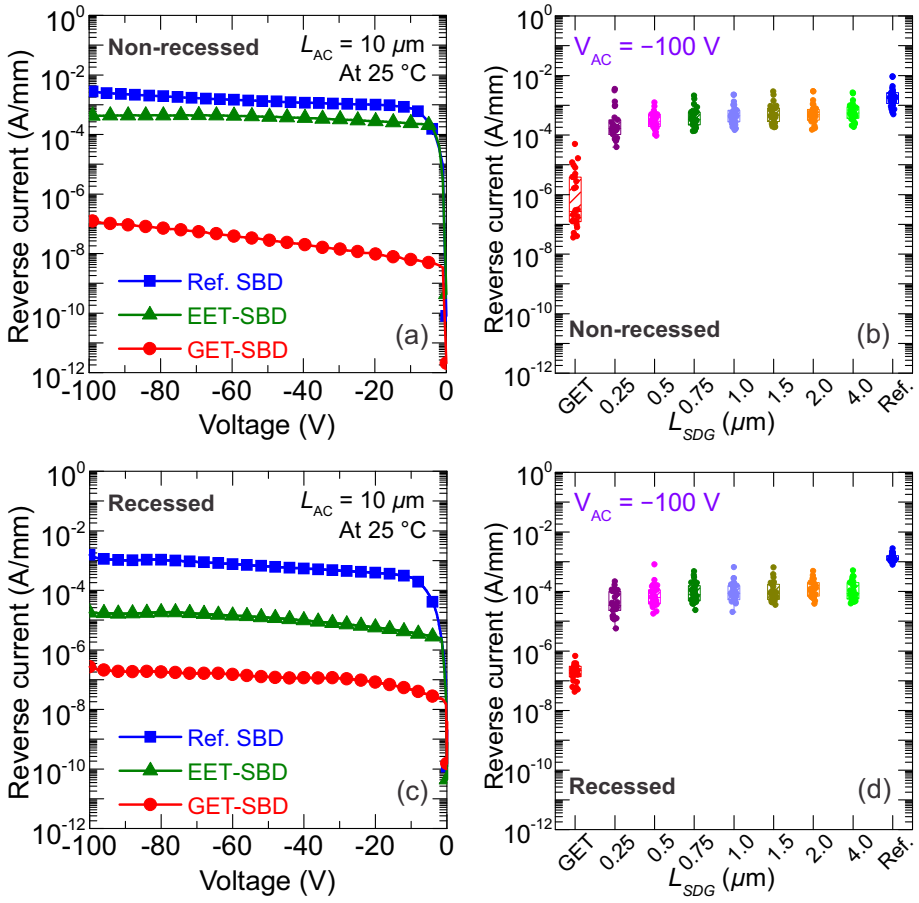


Figure 2.7: (a) Typical off-state characteristics of the reference SBD, non-recessed EET-SBD and non-recessed GET-SBD measured down to −100 V. (b) Box-plot of the leakage current at V_R of −100 V for the reference SBD and non-recessed EET-SBD with different L_{SDG} and GET-SBD. (c) Typical off-state characteristics of the reference SBD, recessed EET-SBD and recessed GET-SBD measured down to −100 V. (d) Box-plot of the leakage current at V_R of −100 V for reference SBD, non-recessed EET-SBD with different L_{SDG} and GET-SBD.

current is dominated by an injection of electrons from the anode to the depleted channel in the lateral direction instead of the vertical direction. Moreover, less spread in leakage is observed in recessed GET-SBDs compared with non-recessed GET-SBDs. As a consequence, the AlGaN barrier recessing is a beneficial technique to

improve the leakage uniformity over the 200-mm wafer without degrading the leakage characteristics.

As speculated in section 2.2.2, the leakage current in the off-state is related to the peak electric field at the corner of the Schottky contact. A TCAD simulation has been performed to visualize the electric field distribution in the AlGaN barrier for the two diode architectures with the same settings as section 2.2.3.2. As shown in Figure 2.8(a), the value of the peak electric field at the corner of the Schottky contact in non-recessed EET-SBDs slightly goes down by reducing the dimension L_{SDG}, a big drop in the peak electric field is achieved with L_{SDG} of 0 μm which is the case for the compact GET-SBD architecture. The inset graph in Figure 2.8(a) shows the zoomed-in electric field distribution in the AlGaN barrier for EET-SBD with different L_{SDG} (from 0.2 to 0.01 μm).

In Figure 2.8(b) the electric field distribution (at V_R of -100 V) along the AlGaN barrier at a distance of 0.5 nm to the anode contact in the GET-SBD is presented. The electric field in Figure 2.8(b) is the module of the electric field vector which is composed of lateral and vertical components. By comparing the vertical and lateral electric field components, we know that the vertical electric field is the more dominant one [45]. As compared with the result from the reference SBD in Figure 2.5(b), the peak value of the electric field at the corner of the Schottky contact drops from 8 MV/cm to $\sim$ 5 MV/cm. There is another peak electric field observed near the Schottky contact in GET-SBD which comes from the redistribution of the electric field from the embedded edge termination. As the reverse voltage increases, the electric field is re-distributed in the access region without significantly increasing the peak electric field at the anode edge (in Figure 2.8(b)). From simulations and experimental results shown above, we can conclude that the leakage current is highly dependent on the peak electric field located at the corner of the Schottky contact, embedding the edge terminations inside the anode trench is an efficient way enabling a reduction of the peak electric field and a suppression of the leakage current. Another point is that the leakage of the GET-SBD features as well a perimeter-effect due to the present of an electric field peak at the anode edge.

2.4 AlGaN Barrier Recess for Forward Current Improvement

2.4.1 Electrical Results and Discussion

The goal of this section is to investigate the impact of AlGaN barrier recess on the forward characteristics of the GET-SBD which has demonstrated a low leakage current independent of the barrier recess process in Figure 2.7.

As reported in the work by Ref. [9, 12, 42], the 2DEG density is related to the AlGaN thickness. By recessing the AlGaN barrier (in Figure 2.4), the 2DEG density reduces, which can shift the threshold voltage in the positive direction [46]. This approach has attracted a lot of attention to achieve enhancement-mode GaN HEMTs [46–49].

An atomic layer etching (ALE) process, as the counterpart to atomic layer deposition (ALD), has been developed by many research groups to allow the removal of the

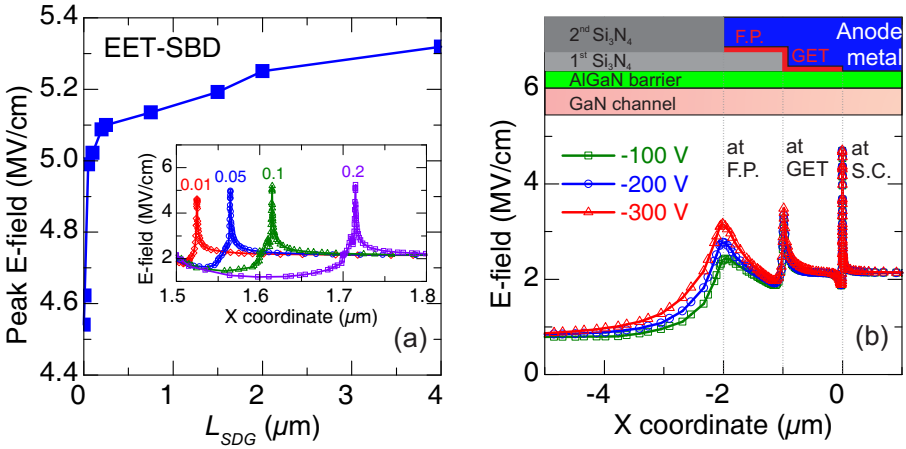


Figure 2.8: (a) The peak value of the E-field (at V_R of −100 V) at the anode edge as a variation of the layout parameter L_{SDG}. The inset graph shows the electric field distribution (at V_R of −100 V) along the AlGaN barrier layer for different L_{SDG} (from 0.2 to 0.01 μm), the peak position corresponds to the anode edge. (b) The electric field distribution along the AlGaN barrier layer for the GET-SBD architecture simulated at different reverse voltages.

AlGaN barrier with controlled accuracy [47, 50]. The ALE process consists of a sequential reaction and removal of the material. We used O_2/BCl_3 chemistry for the ALE process to perform AlGaN barrier recess (*courtesy: ir. B. De Jaeger and process engineers in the p-line, imec*) with controlled accuracy (i.e. ∼1 nm per ALE cycle). In literature, AlGaN partial or full AlGaN barrier recess has been reported to improve the turn-on characteristics [31, 51]. As shown in the inset graph of Figure 2.9(a), the recessed GET-SBD at the anode region is presented. After the opening of the Si_3N_4 passivation layer, a partial removal of the AlGaN barrier was performed by the dry-etching. Consequently, a 5-nm AlGaN barrier is left in the anode region.

In Figure 2.9(a) and (c), the on-state characteristics of non-recessed and recessed GET-SBDs are shown for comparison. In the semi-log scale plot in Figure 2.9(a), a clear shift of the turn-on characteristics of the recessed GET-SBD is observed resulting in a reduction of the turn-on voltage (at a current level of 1 mA/mm [51]). In Figure 2.9(b), the statistical plot of the turn-on voltage (V_T) for the non-recessed and recessed GET-SBDs is shown. With this partial AlGaN barrier recess, the median value of the V_T for the GET-SBD reduces from 0.60 V to 0.42 V. In the linear scale plot of Figure 2.9(c), we observe the reduction of the forward voltage V_F (at a current level of 100 mA/mm [51]) by performing AlGaN barrier recess. This results in the reduction of V_F from 1.45 V to 1.15 V, as is shown in Figure 2.9(d). It is important to note

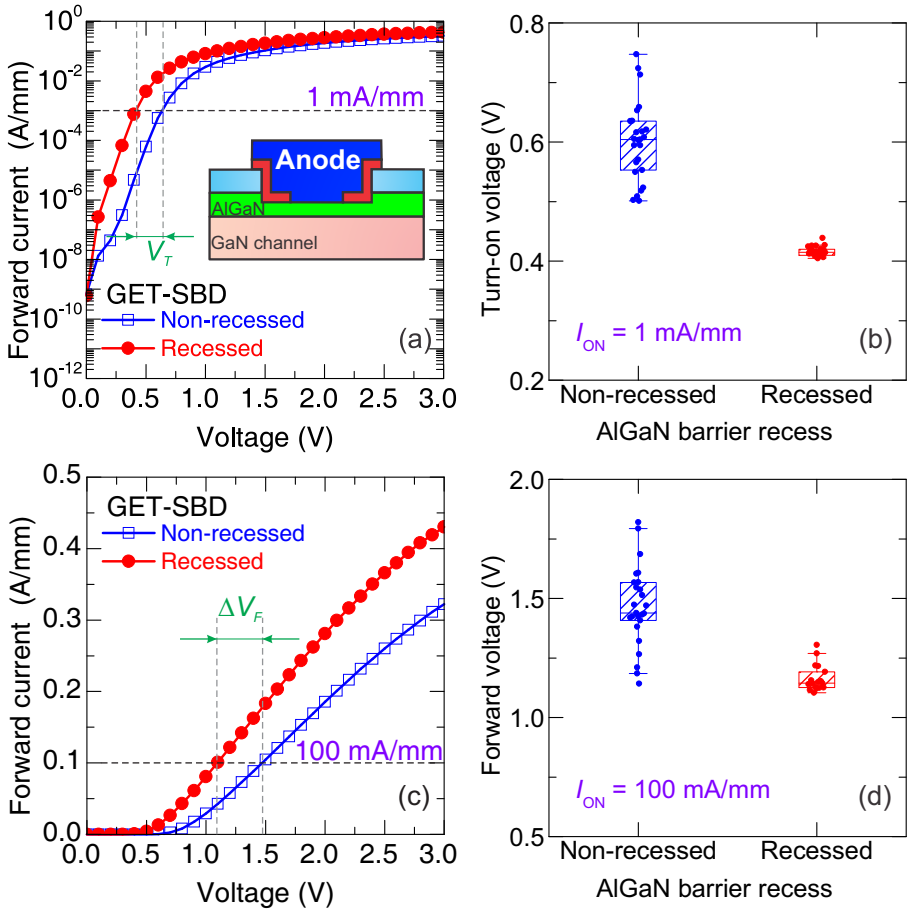


Figure 2.9: Typical forward characteristics of non-recessed and recessed GET-SBD (L_{AC} = 10 μm) in semi-log scale (a) and in linear scale (c). A box plot showing the reduction of turn-on voltage (b) and forward voltage (d) in the recessed GET-SBDs.

that the spread of V_T and V_F is reduced with AlGaN barrier recess. When the AlGaN barrier is not recessed, it is possible that trap-assisted-tunneling current is the dominant process determining the turn-on characteristics. When anode recessing is applied, the electrons from the GaN channel can directly tunnel through the remaining thin AlGaN barrier. In this case, the influence of the trap (probably in the AlGaN barrier layer) on the turn-on characteristics of the recessed GET-SBD is minimized resulting in the spread reduction. The improved forward characteristics can reduce the on-state power loss where high current is flowing in the diodes, thus a more efficient GaN diode can

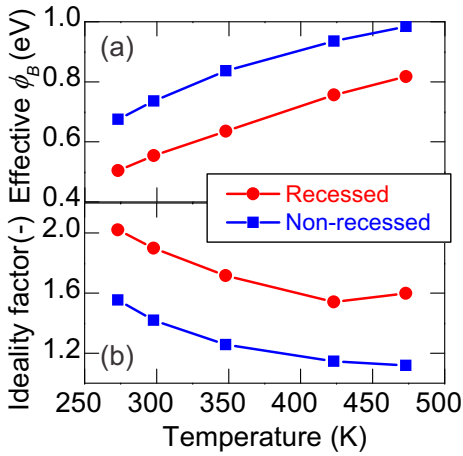


Figure 2.10: The extracted apparent barrier height (a) and ideality factor (b) of non-recessed and recessed GET-SBDs at different temperatures.

be made.

2.4.2 Forward Analytical Modeling

In the forward operation of the AlGaN/GaN SBD, the current flow is due to the transport of electrons from the 2DEG to the anode contact. The transport mechanism can be thermionic emission (TE) of majority carriers over the barrier, electron tunneling (TU) through the barrier or a trap-assisted tunneling (TAT) process. It is most likely that mixed current transport mechanisms are involved. In this section, the impact of the AlGaN recess on the diode parameters (apparent barrier height and ideality factor) will be studied based on the TE model, the tunneling component is described as a lower effective barrier height and a higher non-ideality factor.

According to the theory of thermionic emission mechanism, the forward current density of the diode can be expressed as

$$J_{TE} = A^* T^2 \exp(\frac{-\phi_B}{kT}) \left\{ \exp\left[\frac{q(V - IR_{ON})}{nkT} \right] - 1 \right\}, \tag{2.1}$$

where A^*, ϕ_B, n, R_{ON} are the Richardson constant of AlGaN, Schottky barrier height, ideality factor, and on-resistance. In the ideal case (no Fermi-level pinning at the interface), the barrier height ϕ_B can be defined as follows:

$$\phi_B = \phi_m - \chi_{AlGaN}, \tag{2.2}$$

where ϕ_m and χ_{AlGaN} are the metal work-function and the electron affinity of the

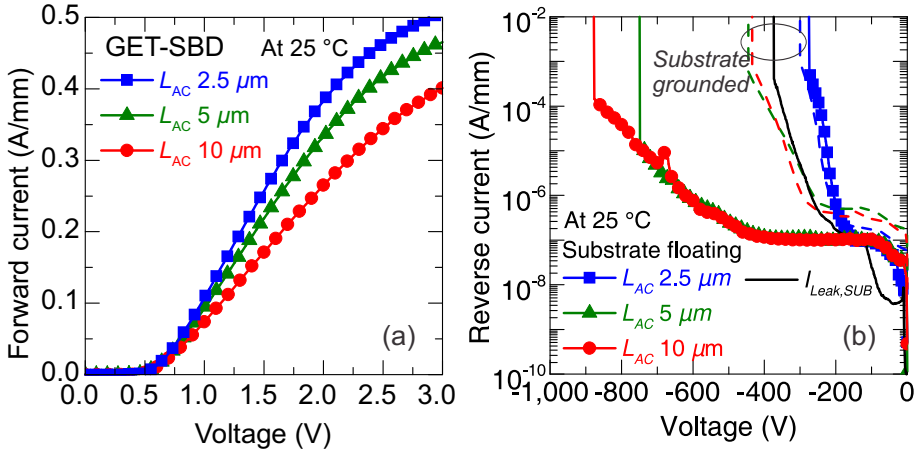


Figure 2.11: (a) The L_{AC} dependent forward characteristics in recessed GET-SBDs. (b) The L_{AC} leakage characteristics in recessed GET-SBDs with both substrate floating and grounding. The substrate leakage current was measured on a separate structure with only a top anode electrode.

AlGaN barrier, respectively. With the ALE process on AlGaN barrier, the metal work-function and AlGaN are assumed to remain the same. Consequently, the barrier height should be independent of the ALE process on the GET-SBD. However, the surface states, dipole charges and surface roughness, etc. can all be changed after the AlGaN recess. The Schottky barrier height will be dependent on the recess conditions. In Figure 2.10(a) and (b), the effective barrier height and ideality factor for non-recessed and recessed GET-SBD at different temperatures are shown. It is seen that the recessed AlGaN/GaN GET-SBD shows a lower effective barrier height than the non-recessed diodes, which explains the improvement of the forward characteristics in Figure 2.9. The lower effective barrier height in recessed GET-SBD is also observed at higher temperatures, which indicates that other current transport mechanisms (i.e. tunneling or trap-assisted tunneling) can play a bigger role in the recessed diodes due to the thinner AlGaN barrier. It is important to note that the ideality factor for both diodes deviates from unity value, especially at relatively low temperatures. As the temperature increases, the ideality factor for both diodes decreases, because more electrons can gain enough thermal energy to overcome the barrier and contribute to the forward current when the TE becomes relatively more dominant. For the non-recessed GET-SBD at high temperature (473.15 K), the ideality factor approaches unity value when the effective barrier height of ∼1 eV was extracted. At high temperature in the GET-SBD with a relatively thick AlGaN barrier, the thermionic emission over the energy barrier dominates over the tunneling component. In this case, the extracted barrier height is closer to the realistic value.

2.5 Breakdown Measurement with Substrate Grounded

From the previous sections, the recessed GET-SBD showed reduced leakage current and improved forward characteristics. The leakage currents in section 2.3.2 were measured with floating substrate, in order to explore the function of the edge termination in the diode intrinsic leakage. For the lateral AlGaN/GaN HEMTs and SBDs fabricated on silicon substrates, the substrate node can be an additional terminal affecting the performance or reliability of the GaN-based lateral devices. As reported in Ref. [52], the substrate bias (floating, grounding, DC voltages) can change the static and dynamic characteristics of the GaN HEMTs. In vertical Si or SiC diodes, the cathode contact is shorted to the substrate due to the intrinsic vertical configuration. In this section, the leakage current of the recessed GET-SBDs (with 3 different L_{AC}) are presented with both floating and grounded substrate to investigate the intrinsic and extrinsic leakage current.

In Figure 2.11(a), the L_{AC} dependence of the forward characteristics of GET-SBDs is shown. It is clear that forward voltage increases with the L_{AC} due to an increased series resistance. In Figure 2.11(b), the leakage current characteristics of GET-SBDs with both substrate floating and grounding configurations are presented. With floating substrate, the breakdown voltage (BV) of the GET-SBD can be improved by using L_{AC} of 5 μm or 10 μm rather than 2.5 μm. When electrically grounding the substrate, a degradation of the leakage current and BV for GET-SBDs (with L_{AC} of 5 μm and 10 μm) is observed in Figure 2.11(b). This indicates that the diode intrinsic leakage (at the AlGaN/GaN surface) is low due to the re-distributed electric field by the edge termination, but the parasitic substrate leakage can play a dominant role in the overall diode leakage current. The substrate leakage current was measured on a separate structure which consists of only a top electrode and bottom substrate, and the substrate leakage is shown in Figure 2.11(b) as well. As the reverse voltage increases, the substrate leakage increases exponentially. This limits the BV of the GET-SBDs to ~400 V. To enable higher voltage (600–1200 V) applications, a more insulating and thicker buffer needs to be designed and used for the diode fabrication. The origin of the buffer leakage and improvement is described in chapter 3.

2.6 Summary and Conclusions

In this chapter, the leakage mechanism in AlGaN/GaN SBDs was firstly analyzed by temperature-dependent off-state characteristics and TCAD electrical simulations. A peak electric field at the anode edge was speculated to be responsible for the high leakage current in conventional AlGaN/GaN SBDs. To reduce the peak electric field, two edge terminations were fabricated in AlGaN/GaN SBDs to suppress the leakage currents. It was demonstrated that embedding the edge terminations inside the anode trench (GET-SBD) has a more effective Schottky contact shielding effect than the EET-SBD, resulting in a significant drop of the leakage current. A correlation of the simulated electric field in EET-SBD, GET-SBD, and conventional SBD with the leakage current was shown in support of this hypothesis. With the ALE process, a partial removal of the AlGaN barrier at the anode region allows for the improvement of

the forward characteristics without the degradation of the low leakage characteristics. Compared with the non-recessed GET-SBD, the recessed GET-SBD showed lower effective barrier height, which was extracted based on the thermionic emission model.

It has been demonstrated that good on-state performance together with low leakage current for AlGaN/GaN diodes can be simultaneously achieved by the design of the device architecture and the process steps. From the statistical evaluation, the recessed GET-SBDs were proven to be a promising device concept obtaining lower forward voltage and less spread in leakage current for high-power switching applications. From the breakdown measurements, it was shown that the parasitic vertical leakage through the AlGaN buffer layers (normally unintentionally doped) can dominate the diode overall off-state characteristics when the reverse voltage exceeds $\sim$300 V. To enable higher voltage applications, a more resistive AlGaN buffer (i.e. carbon- or iron-doped AlGaN) should be designed for the fabrication of AlGaN/GaN diodes.

Chapter 3

Performance Optimization of AlGaN/GaN Diodes with Gated Edge Termination

In this chapter, the leakage current and forward characteristics of Au-free AlGaN/GaN GET-SBDs have been further optimized. This leads to the realization of high performance GaN multi-finger power diodes with total anode width of 10-mm fabricated on 200 mm silicon substrate in Au-free technology.

3.1 Introduction

In efficient power converters, GaN-based SBDs are required to have a low leakage current in the off-state and a low forward voltage drop in the on-state, so that minimal static power loss of the diode can be obtained [35]. AlGaN barrier recess in the anode region has been reported to increase the forward current and lower the forward voltage drop [31, 35]. Furthermore, AlGaN/GaN SBDs with gated ohmic anode structure have been proposed to achieve low turn-on voltages [51]. Various designs of field-plates and edge terminations in lateral and vertical GaN-based SBDs have been reported to suppress the off-state leakage current [35, 53, 54]. Matioli *et al.* [30] presented a lateral AlGaN/GaN SBD with a 3-D anode structure where an integration of a trigate MOS structure with a Schottky junction is designed, demonstrating an ultralow leakage of 260 pA/mm and a turn-on voltage of 0.85 V. Among those promising AlGaN/GaN SBD architectures, typical high work-function (ϕ_m) Ni/Au or Pt-based metals were used for the fabrication of the Schottky contacts [30, 31, 51, 54, 55]. This hinders the high-volume production of those high-performance devices in existing CMOS-compatible processing lines [18].

In the previous chapter, the architecture of the AlGaN/GaN SBD with gated edge termination (GET-SBD) in Au-free technology was demonstrated to show significant diode leakage reduction and good on-state characteristics [29]. A TiN-based metal stack was used as the anode electrode with Ti/Al-based Ohmic schemes. The embedded edge termination in the anode trench enables the reduction of the peak E-field at the anode edge, thus a low leakage current was obtained in AlGaN/GaN SBDs with Au-free technology [35]. Since the Schottky barrier height (SBH ϕ_B) is an important parameter determining the diode characteristics, the ability to tune the work-function of the Au-free anode metals and ϕ_B gives another degree of freedom to optimize the performance of the AlGaN/GaN SBDs [56].

In this chapter, an extensive study of the impact of the anode metal and layout parameters on the diode off- and on-state characteristics has been performed. Two different types of TiN: a standard PVD TiN and a PVD TiN with ionized metal plasma source (IMP TiN), were used as the anode metal in intimate contact with the AlGaN barrier. The IMP TiN with a high-ϕ_m allows for a further reduction of the leakage current of the AlGaN/GaN GET-SBD due to an increased barrier height. The leakage reduction by optimizing the TiN has been confirmed on small diodes (anode width of 100 μm) and multi-finger power diodes (total anode width of 10 mm) at both 25 °C and 150 °C. The diode forward voltage is found to scale down with the reduction of the length of the edge termination without sacrificing the leakage characteristics. This results in a more compact design and a reduction of the capacitance. The benchmarking of the diode off- and on-state parameters (leakage current and forward voltage) shows that our optimized GET-SBDs demonstrate very competitive performances with those of reported lateral AlGaN/GaN SBDs which are mostly fabricated with Ni/Au-based technologies [30, 31, 51, 54, 55].

3.2 Performance Optimization in AlGaN/GaN GET-SBDs

In this section, the optimization of off- and on-state performance of AlGaN/GaN GET-SBDs is performed. As was shown in section 2.5, the parasitic buffer leakage can be dominantly high in the AlGaN/GaN SBDs fabricated on unintentionally doped (UID) buffers. In this section, we first use a carbon-doped AlGaN buffer to effectively suppress the parasitic buffer leakage for a certain voltage range. A further reduction of the leakage current of AlGaN/GaN Schottky barrier diodes with gated edge termination (GET-SBDs) can be achieved by optimizing the TiN as the anode metal. Furthermore, the forward voltage of the GET-SBDs was improved by shrinking the lateral dimension of the edge termination (L_G), which is due to a reduced series resistance. This can result in a more compact design and enable fast switching capability. More in-depth understandings of the off- and on-state operational principles will be shown as well.

3.2.1 Further Leakage Reduction

3.2.1.1 Carbon Doped AlGaN Back Barrier

An AlGaN/GaN/AlGaN double heterostructure (DH) has been grown on 200-mm diameter silicon wafers by metalorganic chemical vapor deposition (MOCVD). The DH-HEMT structure was chosen rather than a single heterostructure because of a better confinement with a raised conduction band of the AlGaN buffer, which showed a reduction of the sub-threshold drain leakage current and an improvement of the punch-through effects of the buffer layer in GaN transistors [11]. However, it was seen in section 2.5 that the buffer leakage of AlGaN/GaN DH Schottky diodes (operating at another quadrant, i.e. anode-to-substrate voltage is highly negative) still dominated the leakage characteristics when the reverse voltage exceeds 300 V. It is likely that the background/auto doping in the buffer makes it relatively conductive rather than insulating. As was reported, the incorporation of Si, O, etc. into the epi-layers during growth is difficult to avoid and can result in an *n*-type AlGaN buffer [57]. The electron

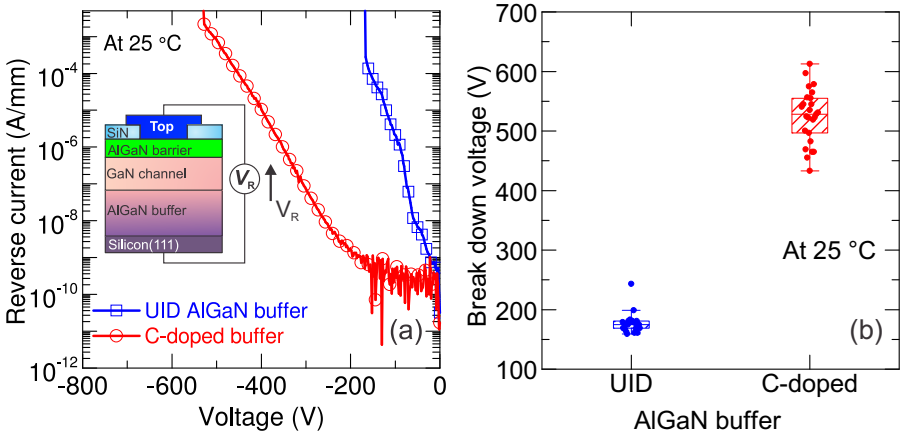


Figure 3.1: (a) Typical vertical breakdown curve for UID and carbon doped buffer. (b) The statistical plot of BV (at leakage current of 5 mA/mm) for UID and C-doped buffer measured at 25 °C.

spilling from the anode contact can then lead to an increased buffer leakage when the buffer is reversely biased.

To enhance the buffer breakdown voltage and suppress the parasitic leakage current through the buffer layers, intentional carbon or iron doping in the (Al)GaN buffer layer has been widely used in literature for RF and power applications [31, 58–60]. The intentional dopants (C or Fe) were reported to introduce trap levels in the band gap of the buffer making it more electrically insulating and bringing the Fermi level to the lower half of the energy band [59]. It was reported that carbon can result in an acceptor level in the (Al)GaN buffer and make the material slightly *p*-type [59].

Unlike Fe doping, carbon doping does not show memory effects during the epitaxial growth [59, 61]. This allows for discontinuous changes of the carbon profile in the doped and un-doped regions [59]. The incorporation of carbon into the buffer can be controlled by growth parameters, i.e. temperature, pressure, and flow rate of the precursor [61, 62]. For the samples studied here, the technique of lowering the growth temperature from 1010 °C to 980 °C was used to intentionally increase the carbon concentration into the buffer. It was reported in Ref. [61] that the carbon concentration can be enhanced by more than 2 orders over a temperature range of 100 °C. The carbon concentration in the $Al_{0.08}Ga_{0.92}N$ buffer layer as the back barrier is $\sim 2\times10^{19}$ cm^{-3} measured by secondary ion mass spectrometry (SIMS). More details regarding the carbon incorporation into the buffer will also be discussed in section 5.2.1 of chapter 5.

An evaluation of the breakdown characteristics of UID and C-doped AlGaN buffer was firstly performed on a vertical breakdown structure shown in the inset graph of

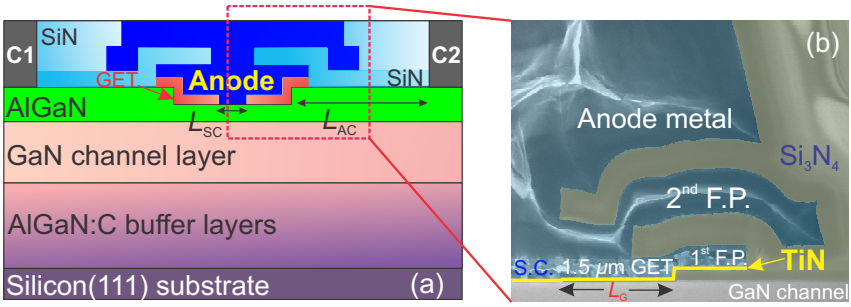


Figure 3.2: (a) The schematic cross-section of the AlGaN/GaN Schottky barrier diode with gated edge termination (GET) and two-level field plates. (b) Cross-sectional SEM image of the anode region in gated edge terminated SBD (GET-SBD). TiN, as the bottom layer of the anode metal stack, is indicated in the picture.

Figure 3.1(a). In Figure 3.1(a), typical breakdown curves at 25 °C are shown. With carbon-doping in the AlGaN buffer as the back-barrier, the vertical parasitic leakage was suppressed by orders of magnitude. The median BV value (defined at a current level of 5 mA/mm) has been enhanced from ∼180 V to ∼530 V by the carbon doping in the AlGaN back-barrier, as is shown in Figure 3.1(b). This buffer can be an interesting candidate for a 200-V application platform. An improvement of the BV and leakage current of the GET-SBD is expected and will be discussed in the following subsection.

3.2.1.2 Optimization of TiN as Anode Metal

A schematic of the AlGaN/GaN SBD with gated edge termination (GET-SBD) is shown in Figure 3.2(a). Two-level anode field plates (F.P.) are fabricated on the Si_3N_4 passivation layers towards the cathode, which was also used in Ref. [55] to achieve high breakdown voltage. A cross-sectional SEM image of the anode region in the GET-SBD is shown in Figure 3.2(b) presenting L_G of 1.5 μm gated edge termination (GET) and 2-level anode metal field plates. The conventional AlGaN/GaN SBD (without edge termination and without AlGaN barrier recess) was also processed as a reference.

Concerning the bottom 20-nm TiN layer (as indicated in Figure 3.2(b)), standard physical vapor deposited (PVD) TiN (at 23 °C) and ionized metal plasma (IMP) PVD TiN (at 350 °C) were used separately on two otherwise identical wafers. The crystallographic orientation of PVD TiN and IMP TiN was examined by the grazing incidence X-ray diffraction (GIXRD) with spectra shown in Figure 3.3(a). It was found that IMP TiN consists dominantly of (200) crystallites (a peak at 42.5°) compared with mixed grain orientations in standard PVD TiN [63]. The different crystallographic orientation can be related to the difference in deposition temperature because metal

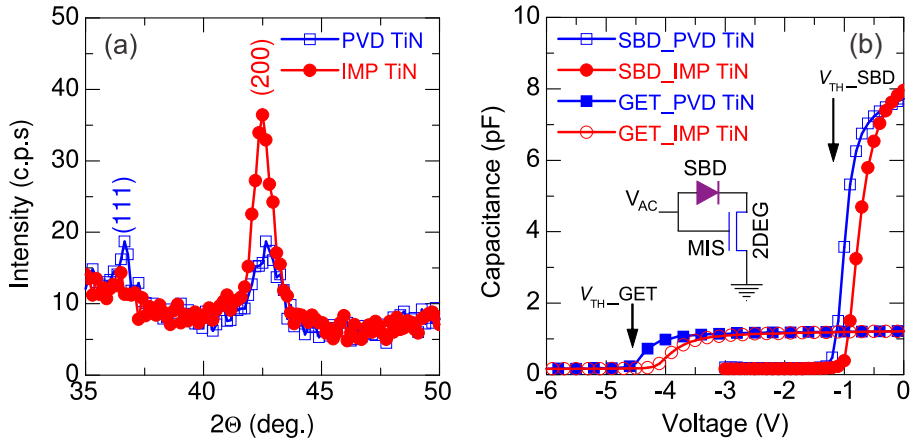


Figure 3.3: (a) Omega-2theta scan of the standard PVD TiN and the ionized metal plasma deposited TiN (IMP TiN). (b) Capacitance–voltage (C–V) measurements on conventional AlGaN/GaN SBD and GET-SBD with IMP TiN and standard PVD TiN, respectively. The $V_{\mathrm{TH,\,SC}}$ of the SBD and $V_{\mathrm{TH,\,MISHEMT}}$of GET-SBD are shifted positively with a value of $\sim$ 200 mV with IMP TiN.

Table 3.1: Deposition details and properties of standard PVD TiN and IMP TiN

	Temperature (°C)	Thickness (nm)	Crystal orientation
PVD TiN	350	20	(200) and (111)
IMP TiN	23	20	(200)

tends to grow in a "preferred orientation" to obtain a stable crystal structure at high deposition temperatures [64]. The deposition details and material properties of these two TiN metals are further summarized in Table 3.1. It was reported that the work-function of metals is dependent on the crystallographic orientation [65]. To evaluate the work-function difference, capacitance–voltage (C–V) measurements have been performed at 100 kHz on conventional AlGaN/GaN SBDs and recessed GET-SBDs with IMP TiN and standard PVD TiN, respectively (in Figure 3.3(b)). The capacitance of the Schottky contact for recessed GET-SBD is missing in Figure 3.3(b), because the 2DEG is fully depleted under the Schottky metal at equilibrium. A positive V_{TH} shift ($\sim$ 200 mV) is observed in the SBD and GET-SBD with IMP TiN compared with devices using PVD TiN. This indicates a higher ϕ_m for IMP TiN compared with standard PVD TiN. It is expected that a higher ϕ_B of AlGaN/GaN SBD can be obtained with IMP TiN as the anode metal. The TiN work-function variation gives the possibility to optimize the diode performances.

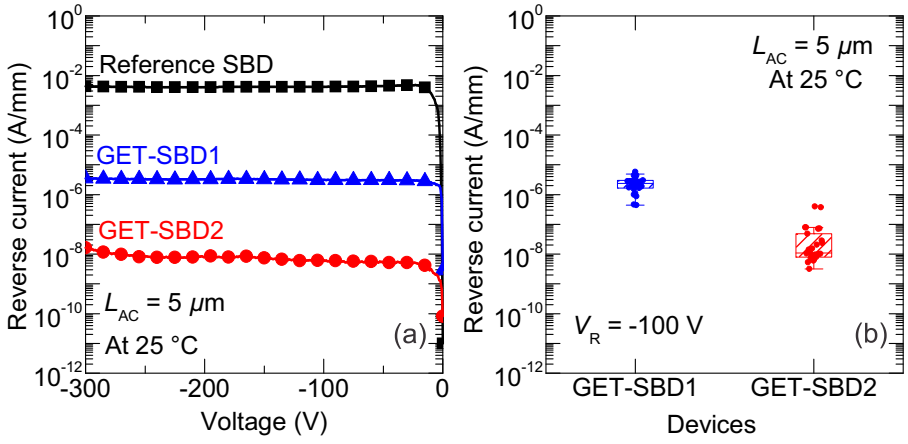


Figure 3.4: (a) Typical off-state characteristics of the GET-SBD (labeled as GET-SBD1) and the one with optimized TiN anode metal (labeled as GET-SBD2) measured down to V_R of −300 V , the leakage of a reference AlGaN/GaN SBD is also shown. (b) The statistical plot of room-temperature leakage current (at V_R of −100 V) for GET-SBD1 and GET-SBD2.

As displayed in Figure 3.4(a), the leakage currents of a conventional SBD, GET-SBD with standard PVD TiN (labeled as GET-SBD1) and GET-SBD with IMP TiN (GET-SBD2) are measured (at 25 °C) down to a reverse voltage (V_R) of −300 V. The conventional AlGaN/GaN SBD (with PVD TiN as the anode metal) suffers from high leakage current due to electron tunneling through the AlGaN barrier layer in the lateral depletion region [35]. In the GET-SBD, the edge termination pinches off the 2DEG channel and redistributes the electric field in the vicinity of the Schottky contact [29, 35]. As has been shown in Figure 3.3(b), the GET structure with 15-nm Si_3N_4 on recessed AlGaN barrier shows a threshold voltage (the voltage to build up the 2DEG channel) of ∼–4.5 V. The more positive threshold voltage in the region of GET, the better electrostatic control of the channel will be. With the same anode metal of PVD TiN, the GET-SBD1 shows three orders of magnitude reduction in leakage compared with the conventional SBD in Figure 3.4(a). By combining a high-ϕ_m IMP TiN and an edge termination in GET-SBD2, a higher SBH and lower E-field can be obtained simultaneously resulting in a stronger blocking capability for the leakage. This yields a 5 to 6 orders of magnitude leakage reduction compared with the conventional AlGaN/GaN SBD with PVD TiN. In Figure 3.4(b), the statistical leakage value over the 200-mm wafers (at V_R of −100 V) of GET-SBD1 and optimized GET-SBD2 with IMP TiN is shown. It confirms that the leakage current can be further reduced with a high ϕ_m IMP TiN as the anode metal. The optimized GET-SBD2 shows a median leakage value of 10.8 nA/mm comparing with 2.39 μA/mm in the case of

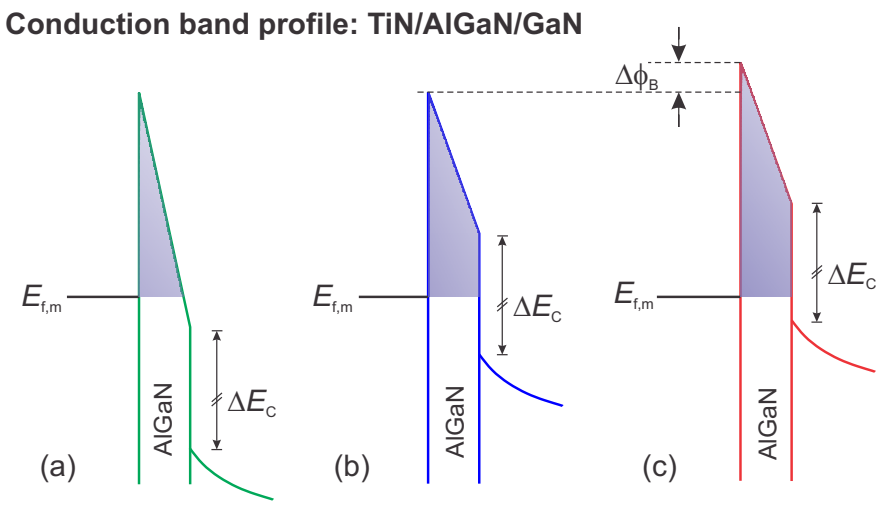


Figure 3.5: The schematics of the conduction band profile of a reversely biased TiN metal/AlGaN barrier/GaN channel for the reference SBD (a), the GET-SBD1 (b), and the GET-SBD2 (c).

GET-SBD1 with the standard TiN as the anode metal.

The different leakage characteristics of reference SBD, GET-SBD1 and GET-SBD2 can be further interpreted from the band diagram. As shown in Figure 3.5, the schematic band diagrams (at the anode edge) of reference SBD, GET-SBD1 and GET-SBD2 at the same reverse voltage are shown, respectively. The reference SBD suffers from a peak electric field at the anode edge, that leads to a severe band bending in the AlGaN barrier shown in Figure 3.5(a). The electrons from the anode electrode have the tendency to tunnel through the AlGaN energy band due to a narrowed energy band. The tunneling probability is related to the shaded area, according to the WKB approximation which relates the tunneling probability to the energy barrier profile [66].

With a gated edge termination in the GET-SBD architecture, the electric field at the anode edge is reduced resulting in an alleviated band bending. As shown in Figure 3.5(b), it illustrates the conduction band profile for GET-SBD1 with PVD TiN anode metal. In comparison with the reference SBD with PVD TiN anode metal in Figure 3.5(a), the physical barrier height remains the same in GET-SBD1. However, the shaded area is larger due to a reduced field in the AlGaN barrier layer. This reflects in the significant leakage reduction in Figure 3.4(a), because the leakage current is exponentially dependent on the energy barrier profile. By using IMP TiN as the anode metal, its higher work-function results in a higher Schottky barrier height in GET-SBD2 comparing with GET-SBD1. Assuming that the electric field in the AlGaN for GET-SBD1 and GET-SBD2 is the same, the increased barrier height leads to a further

increase of the shaded area and a reduction of the leakage current.

To evaluate the breakdown voltage (BV), off-state measurements on both GET-SBD1 and optimized GET-SBD2 with a variation of anode-to-cathode spacing L_{AC} (from 1.5 μm to 10 μm) are performed with the substrate electrically grounded. As presented in Figure 3.6(a), the diode leakage current (prior to the diode breakdown or buffer breakdown) is independent of L_{AC} in both GET-SBDs due to the function of the gated edge termination to pinch-off the channel. This observation is different from the results reported in Ref. [51,67] where L_{AC} dependent leakage characteristics were shown. The reason can be due to the function of the embedded edge termination. Without effective edge termination, the peak electric field at the Schottky contact corner increases with reverse voltage due to extended lateral depletion region. This typically results in an increasing leakage with reverse voltage [67]. With a gated edge termination, the GET-SBD1 and GET-SBD2 show negligible dependence on the reverse voltage and L_{AC}. In the case of our GET-SBDs, the scaling down of L_{AC} will allow for the reduction of series resistance and forward voltage without degrading the leakage characteristics. The difference in leakage current between the GET-SBD1 and optimized GET-SBD2 is further shown in Figure 3.6(a), and the BV of these two GET-SBDs with identical L_{AC} appears to be the same, driven by the same breakdown mechanism.

In Figure 3.6(b) and (c), the statistical BV values (when the leakage reaches 5 mA/mm) of GET-SBD1 and GET-SBD2 with L_{AC} variations are shown. With the increase of the L_{AC} dimension (from 1.5 μm to 5 μm), there is a linear increase ($\sim$ 120 V/μm or 1.2 MV/cm) of the BV observed in both structures. From theoretical calculations, the critical electric field for hexagonal GaN was reported to be $\sim$3.3 MV/cm [68–70]. This BV mechanism (GET-SBD with L_{AC} from 1.5 μm to 5 μm) is triggered in the AlGaN/GaN active layers in the vicinity of the anode contact where a peak electric field is present. The enhancement of the electric field at the anode region results in a lower breakdown voltage compared to the physical limitation of GaN material. With a further increase of the L_{AC} dimension from 5 μm to 10 μm, however, it does not lead to a further enhancement of BV shown in Figure 3.6(b) and (c). This is due to the buffer breakdown in the vertical direction where the electric field increases vertically as the reverse voltage increases. As can be also seen in Figure 3.6(a), the buffer leakage current (measured on a separate structure with top anode contact and the bottom silicon substrate) increases exponentially with the reverse voltage.

In Fig. 3.7(a), the electric field distribution in the AlGaN barrier (0.5 nm away from the contact) was simulated in TCAD for the GET-SBD with a variation of the 2nd F.P.. The electric field is more uniformly distributed in the access region, however, the peak electric field at the Schottky contact (S.C.) does not change with an implementation of the 2nd F.P. structure. In Fig. 3.7(b), the breakdown characteristics of GET-SBD1 and GET-SBD2 (L_{AC} of 5 μm) are presented for devices with and without 2nd F.P.. The buffer leakage currents were monitored simultaneously during the measurements. It is seen that the leakage value prior to breakdown is independent on the 2nd F.P. for GET-SBD1 and GET-SBD2. This can be explained by the TCAD simulation in Fig. 3.7(a) showing an unchanged peak E-field at the anode edge. When reverse voltage exceeds 400 V, the buffer leakage becomes more dominant than the leakage of the diode. It

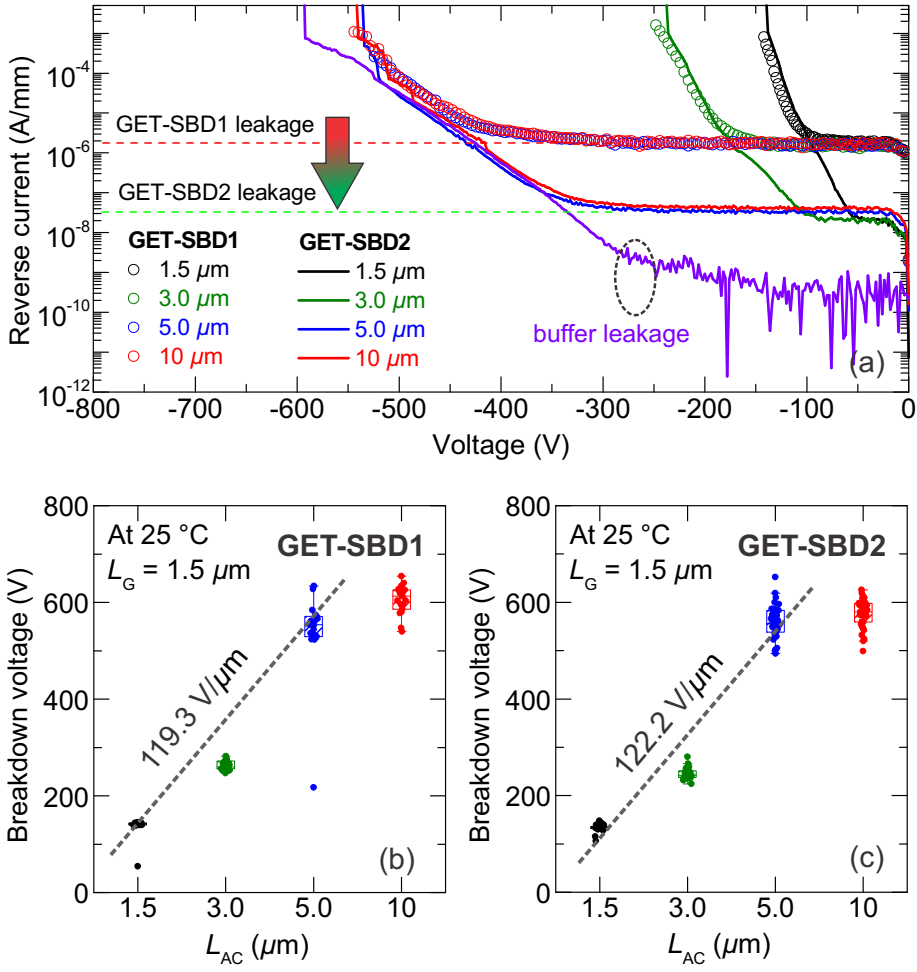


Figure 3.6: (a) Typical leakage and breakdown characteristics of the GET-SBD1 and optimized GET-SBD2 with a variation of anode-to-cathode spacing L_{AC}. The buffer leakage current was measured on a separate structure with only the top anode contact and the substrate. The statistical plots of BV (at current level of 5 mA/mm) in GET-SBD1 and optimized GET-SBD2 with 4 different L_{AC} are shown in (b) and (c), respectively.

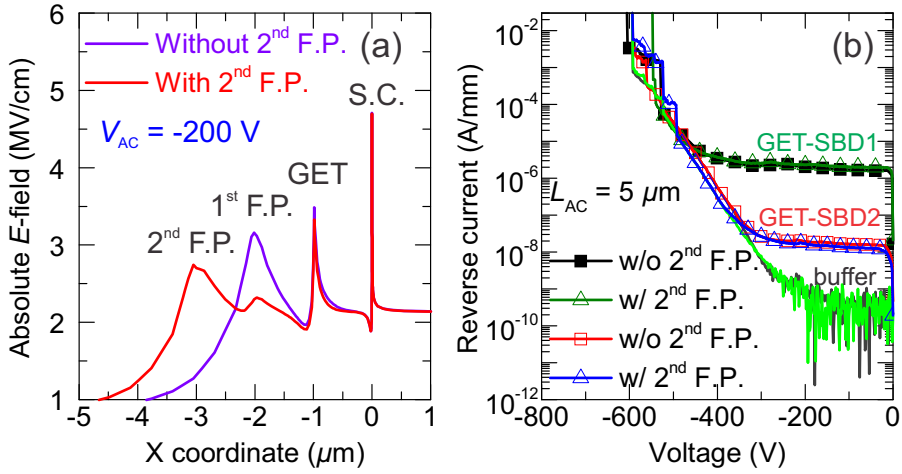


Figure 3.7: (a) TCAD simulation of electric field distribution in AlGaN barrier (0.5 nm away from the anode contact) at −200 V. (b) Breakdown characteristics of GET-SBD1 and GET-SBD2 with variation of 2nd F.P., the buffer leakage currents were monitored during the measurements.

further confirms that the buffer breakdown of the GET-SBD is the limiting factor for its high-voltage operations.

The observation of two distinct breakdown mechanisms has also been previously identified in GaN HEMTs [71]. It indicates that the buffer breakdown can be the limiting factor when the reverse voltage exceeds a critical value (depending on the buffer quality and thickness, etc.). For the GET-SBD with L_{AC} of 5 μm, the diode shows excellent performance for 200-V applications. Further buffer design optimization is needed to boost the buffer breakdown voltage.

3.2.2 Forward Optimization

As is shown in the previous section, the GET-SBD with the high-ϕ_m IMP TiN is shown to be a promising candidate for low-leakage applications. However, it is also important to evaluate the on-state characteristics of the GET-SBDs with the 2 different TiN variations. Normally, a Schottky diode with a high metal work-function results in a high turn-on voltage. That explains why reported Ni/Au-based AlGaN/GaN Schottky diodes typically show higher turn-on voltages than those of Au-free AlGaN/GaN diodes [30, 32]. A model for the forward conduction will be developed to obtain more insights in the current transport mechanisms based on new information of our material properties.

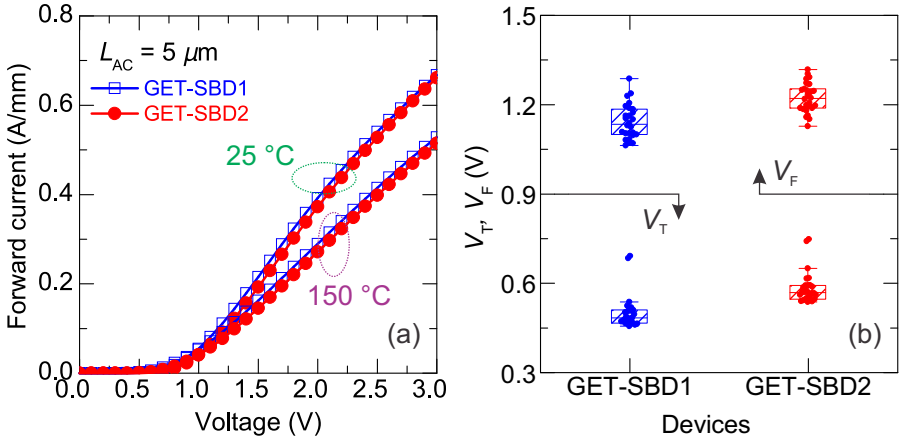


Figure 3.8: (a) Typical forward characteristics of GET-SBD1 and GET-SBD2 at both 25 °C and 150 °C. (b) The statistical plot of turn-on voltage V_T (at forward current of 1 mA/mm) and forward voltage V_F (at forward current of 100 mA/mm) for GET-SBD1 and GET-SBD2 at 25 °C.

3.2.2.1 Forward Characteristics and Modeling

The typical forward characteristics of GET-SBD1 and GET-SBD2 at both 25 °C and 150 °C are presented in Figure 3.8(a). Even though the two GET-SBDs have a different work-function TiN, the difference in their on-state characteristics appears to be small. The statistical values of turn-on voltage V_T (at forward current of 1 mA/mm) and forward voltage V_F (at forward current of 100 mA/mm) for GET-SBD1 and GET-SBD2 are shown in Figure 3.8(b). The median values of V_F for GET-SBD1 and GET-SBD2 are 1.14 V and 1.22 V, respectively. Though the anode metal IMP TiN has a higher ϕ_m, no severe degradation of on-state characteristics of GET-SBDs is observed. By using the formula describing the thermionic emission (TE) mechanism, the values of effective Schottky barrier height ϕ_B for GET-SBD1 and GET-SBD2 can be extracted to be 0.59 eV and 0.68 eV, respectively. The ideality factor values are 1.30 and 1.23 for GET-SBD1 and GET-SBD2, respectively. Besides the process of the injection of majority carriers over the Schottky barrier, there might be other current transport mechanisms (i.e. tunneling, trap-assisted tunneling, etc.) contributing to the on-state currents [72, 73].

From literature in [73], the forward current transport mechanisms of an AlGaN/GaN Schottky diode can be electron tunneling (TU) through the barrier besides the thermionic emission process. The forward current density of the tunneling mechanisms can be expressed as

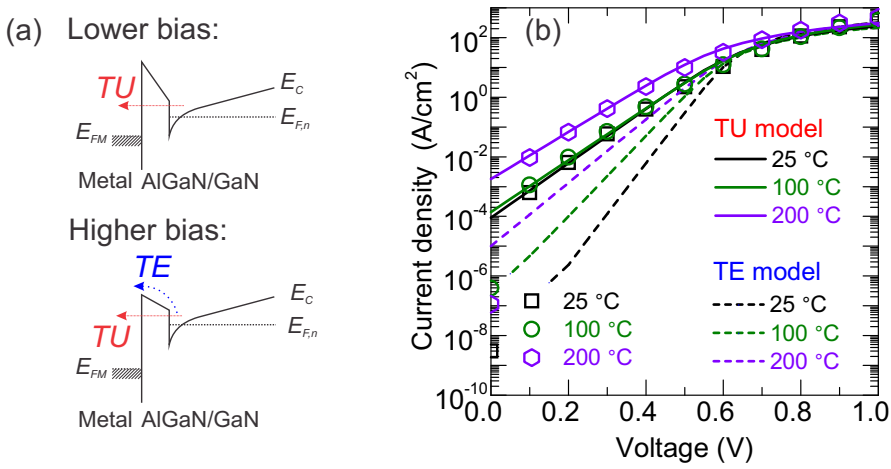


Figure 3.9: (a) Conduction band profile of AlGaN/GaN diode under different bias conditions illustrating the dominant current transport mechanisms in the device. (b) A forward modeling on the measurement data (from AlGaN/GaN SBD with PVD TiN) based on analytical equations of TU and TE mechanisms.

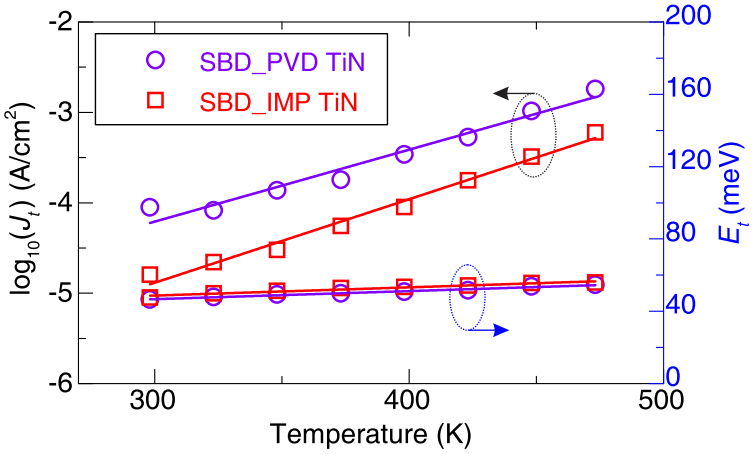


Figure 3.10: Temperature dependence of tunneling saturation current J_t and tunneling energy E_t for AlGaN/GaN SBD and GET-SBD with PVD TiN and IMP TiN, respectively.

$$J_{TU} = J_t \left\{ \exp\left[\frac{q(V - IR_{ON})}{E_t} \right] - 1 \right\}, \tag{3.1}$$

where J_t and E_t are the tunneling saturation current and the tunneling energy which is related to the tunneling barrier profile. To gain more understanding of the forward current transport in our devices, analytical equations of TE and TU mechanisms were used to model the measurement data at three different temperatures (in Figure 3.9(b)). An excellent agreement between the measurement data and the current-transport expression for tunneling process at three different temperatures is shown. The TE mechanism with ideality factor n of unity only starts to become comparable with the tunneling current when the diode is already at an appreciable forward bias. Additionally, we observed an exponential dependence of the tunneling saturation current on the temperature (shown in Figure 3.10). The direct tunneling process is, in principle, temperature independent. This suggests a trap assisted tunneling (TAT) process in our diodes. Arslan *et al.* and Donoval *et al.* reported that a dislocation-governed transport mechanism is the dominant process in the forward operation of GaN/AlGaN/GaN and InAlN/GaN diodes [72, 73] when the dislocation density is $\sim 10^9$ cm^{-2} [73]. According to the model of dislocation-governed tunneling mechanism in Schottky diodes [73, 74], the tunneling saturation current density J_t at zero absolute temperature can be described by

$$J_t(0\ K) = q \times \nu_D N_{dis} \exp\left(-q\Phi_B / E_t\right), \tag{3.2}$$

where ν_D is the Debye frequency ($\nu_D \approx 1.68 \times 10^{13}$ s^{-1} for $Al_{0.25}Ga_{0.75}N$ barrier and

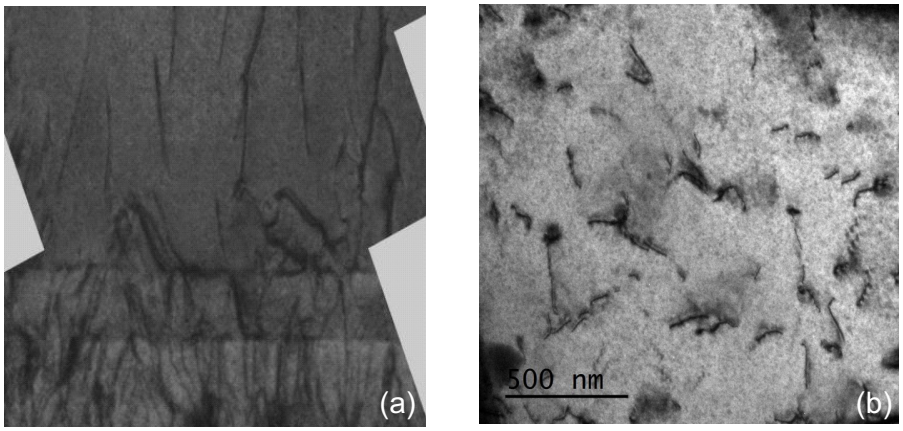


Figure 3.11: (a) Cross-section TEM image of GaN/AlGaN epitaxial layers grown on a silicon substrate by MOCVD. A stack of AlGaN buffer layers with different Al percentage is normally used to reduce the dislocation density in AlGaN/GaN active layers. (b) A typical plan-view TEM micrograph acquired along the $\langle 1\bar{2}1\bar{3}\rangle$ zone axis. All types of threading dislocations are visible under this imaging condition.

N_{dis} is the dislocation density (DD) in the space charge region, and Φ_B is the barrier height.

Table 3.2: The extracted values of J_t, E_t at 0 K, and the calculated ϕ_B for 4 devices according to equation (4.1), and n extracted from TE model are listed for comparison.

Device	J_t (0 K) (nA/cm^2)	E_t (0 K) (eV)	ϕ_B (eV)	n (-)
SBD_PVD TiN (non-recessed)	254	0.033	0.81	1.53
SBD_IMP TiN (non-recessed)	17	0.037	1.01	1.31
GET_PVD TiN (recessed)	159	0.0031	0.08	1.30
GET_IMP TiN (recessed)	0.83	0.0042	0.13	1.23

Based on this theory, the barrier height of our Au-free AlGaN/GaN diodes can be evaluated with the additional information of dislocation density. Due to the heterogeneous epitaxial growth of (Al)GaN layers on silicon substrate, an increased number of crystal defects can be generated. In Figure 3.11(a), the vertical threading

dislocation in the epi-layers can be visualized in a cross-sectional TEM image. The dislocation density can be gradually reduced by changing the Al percentage in the AlGaN buffer layers and by modifying the growth conditions. It is still possible that some dislocation can propagate and exist in the active AlGaN barrier and GaN channel which can affect the transport mechanisms in both on- and off-state operations [75]. Figure 3.11(b) shows a typical plan-view transmission electron microscopy (TEM) micrograph of our AlGaN/GaN/AlGaN buffer stack. The image was taken along the $\langle 1\bar{2}1\bar{3}\rangle$ zone axis. In such an image, all screw, edge, and mixed types of threading dislocations are revealed [76]. The threading dislocation density was estimated statistically by averaging its value obtained from several such planar view TEM micrographs acquired at different location of the TEM specimen. The dislocation density in our AlGaN/GaN structures is estimated to be $\sim 4 \times 10^9$ cm^{-2} which is consistent with the values (10^8–10^{10} cm^{-2}) reported in literature for AlGaN/GaN structures grown by MOCVD on silicon.

The temperature dependence of J_t and E_t for SBD_PVD TiN and SBD_IMP TiN is shown in Figure 3.10. The tunneling saturation current shows an exponential dependence on the temperature, while tunneling energy is weakly temperature-dependent. The J_t and E_t at 0 K for the four devices under study can be extrapolated and used for the calculation of the Schottky barrier height, as are displayed in Table 3.2. The n is the ideality factor extracted according to thermionic emission model at room temperature. The ϕ_B of SBD_PVD TiN and SBD_IMP TiN is calculated to be 0.81 and 1.01 eV, respectively. The difference in ϕ_B between two SBDs is 0.20 eV which matches the results obtained from V_T shift ($\Delta\ \phi_B = q \times \Delta\ V_T$) in Figure 3.3. The recessed GET-SBDs should have the same barrier height as the SBDs (with the same anode metal), however, a much lower E_t and a much lower ϕ_B are extracted. This indicates that direct tunneling and field emission of carriers through the thin AlGaN barrier can be important additional mechanisms in the recessed diodes. The ideality factors are deviating from unity for all diodes, since the TE mechanism is not the dominant transport process for both non-recessed and recessed AlGaN/GaN SBDs.

3.2.2.2 L_G Scaling

The gated edge termination (with lateral dimension L_G) in the GET-SBD allows for the redistribution of the electric field and the pinching-off of the 2DEG channel, thus low leakage current has been obtained. It is important to note that the dimension of L_G contributes to the capacitance and the on-state resistance. Therefore, the capacitance–voltage (C–V) measurements have been performed at 100 kHz on GET-SBD2 with different L_G. As shown in Figure 3.12, by scaling down L_G, the capacitance reduces linearly resulting in a more compact configuration. This can potentially improve the switching capability and allows for the improvement of on-state characteristics in GET-SBD2. As expressed in Equation 3.3 below, the forward voltage linearly scales with the L_G dimension at forward current of 100 mA/mm.

$$V_F = V_T + R_{ON} \times I_{ON} = V_T + (R_{ACCESS} + \rho \times L_G/A) \times I_{ON}. \tag{3.3}$$

In Figure 3.13(a) and (b), typical off-state and on-state characteristics of GET-SBD2

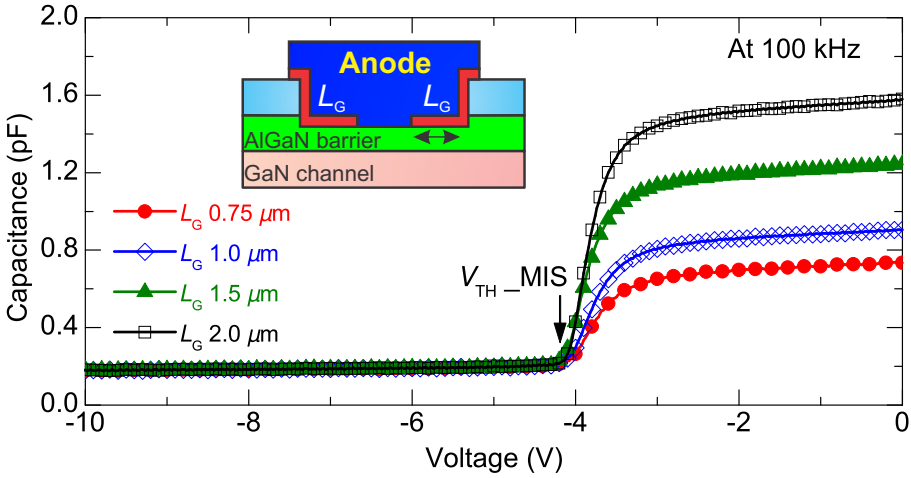


Figure 3.12: *C–V* measurements on GET-SBD2 with L_G variations measured at 100 kHz. The inset schematic structure shows the anode region of the GET-SBD.

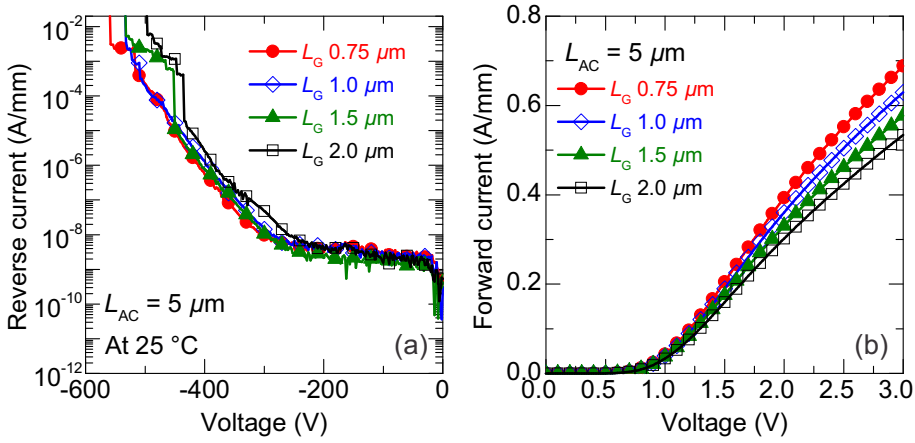


Figure 3.13: Typical off-state (a) and on-state (b) characteristics of the GET-SBDs with different L_G dimensions.

(with L_{AC} of 5 μm) with different L_G are shown. The leakage characteristics of GET-SBDs show no degradation by scaling down L_G, while an improvement in forward characteristics is observed (shown in Figure 3.13(b)) due to reduced series resistance.

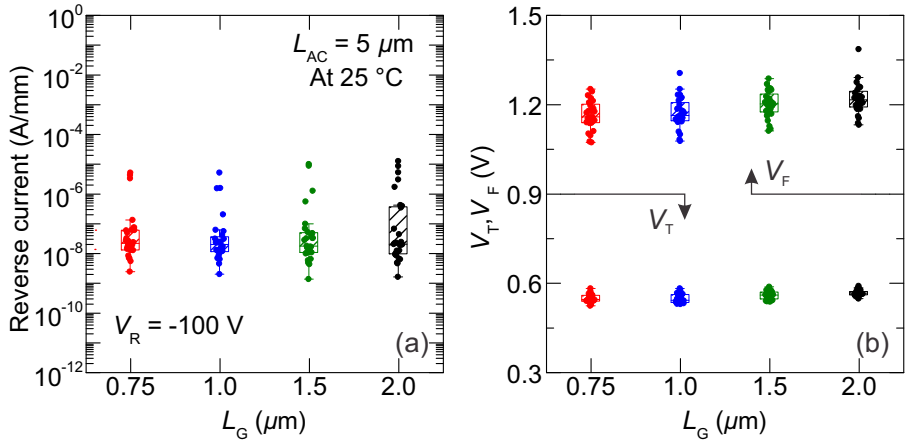


Figure 3.14: (a) Statistical plot of leakage current at V_R of −100 V. (a) Statistical values of V_T and V_F for GET-SBDs with a variation of L_G dimensions.

The statistics of leakage and on-state voltages are presented in Figure 3.14(a) and (b), respectively. By scaling down L_G from 2 μm to 0.75 μm, the leakage current is invariant and maintains a low value of ∼10 nA/mm. However, the leakage is shown to be high (in Figure 3.4(a)) when L_G is 0 μm which is the case for conventional AlGaN/GaN SBD, so there is a limit to further reduce L_G without further increasing the leakage current. From the statistics of on-state voltages, the turn-on voltage does not change with L_G because the V_T is mostly determined by the barrier height and transport mechanisms. A slight improvement of forward voltage is shown in Figure 3.14(b). The median value of the forward voltage reduces from 1.22 V to 1.16 V by scaling down the L_G from 2.0 μm to 0.75 μm. This can reduce the on-state power loss when high forward current is flowing through the diodes.

From the results shown in Figure 3.14, a leakage current of ∼10.0 nA/mm and a forward voltage of 1.16 V have been achieved in GET-SBD2 (with IMP TiN) with L_G of 0.75 μm. Shrinking L_G allows for further optimization of the on-state characteristics and a more compact design for GET-SBD architecture based on Au-free GaN-on-Si technology.

3.2.3 Benchmarking

In this section, we benchmark earlier reported AlGaN/GaN lateral Schottky barrier diodes and this work (both Au-free and Ni/Au-based technologies) in terms of leakage current (at V_R of −200 V, leakage value from Ref. [30] was taken at −127 V) and forward voltage (at a forward current of 100 mA/mm). The leakage and forward voltage can be both L_{AC} dependent, thus several points from the same published

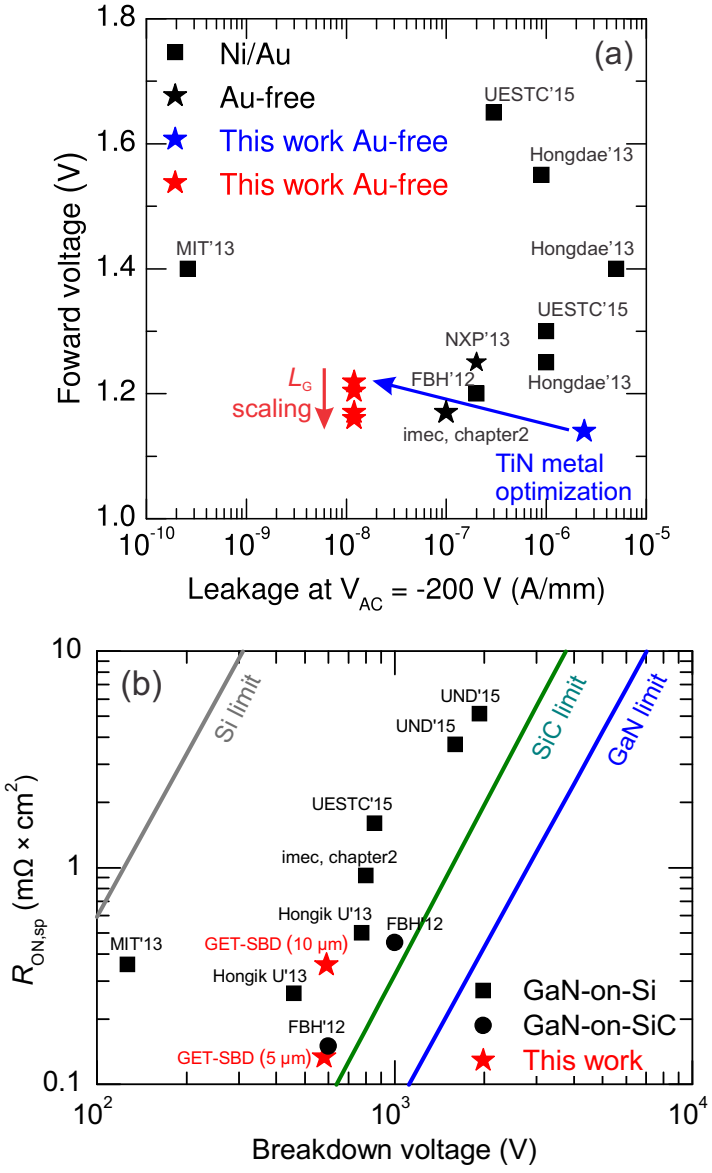


Figure 3.15: (a) Benchmarking the leakage current and forward voltage of lateral AlGaN/GaN Schottky diodes with Ni/Au and Au-free technology. (b) Benchmarking the breakdown voltage and specific on-resistance of lateral AlGaN/GaN on silicon and silicon carbide (SiC) substrate.

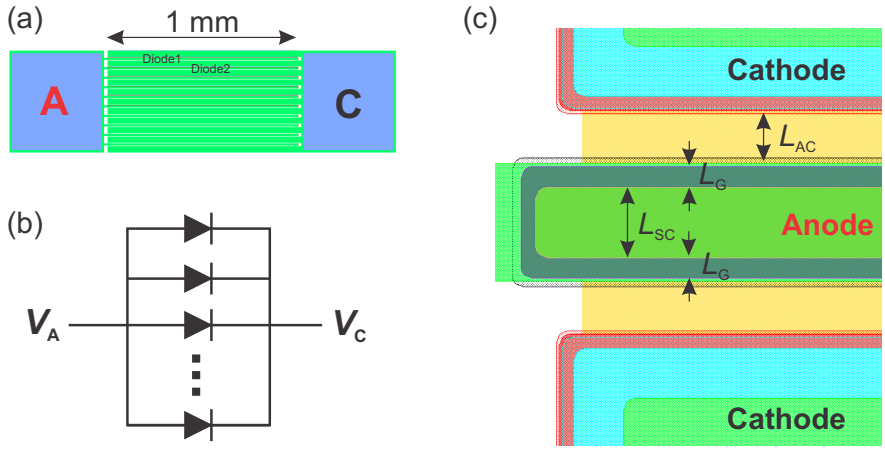


Figure 3.16: (a) A top review of multi-finger GET-SBD power diodes. There are 10 GET-SBDs in parallel, each GET-SBD has an anode finger width of 1-mm. (b) The equivalent circuit symbol for the power diodes. (c) A top view of a single finger GET-SBD.

work can be found in the benchmarking plot. As shown in Figure 3.15(a), most of the reported AlGaN/GaN SBDs were fabricated by using Ni/Au or Pt-based anode metal stacks which are not compatible with Si-based processing lines. Our Au-free AlGaN/GaN GET-SBDs with the optimized TiN metal exhibit low leakage current of ~10 nA/mm. The performance is competitive over most reported data. By scaling down the L_G parameter, the forward voltage can be further reduced without degradation of off-state characteristics. This work, to the best of our knowledge, leads to lateral AlGaN/GaN SBDs with the best performance in terms of low leakage and low forward voltage. Moreover, excellent characteristics have been demonstrated for AlGaN/GaN SBDs fabricated on 200-mm silicon substrate and realized by fabrication in a CMOS-compatible process line.

In Figure 3.15(b), the benchmark plot of BV versus $R_{ON,SP}$ for lateral AlGaN/GaN SBDs on Si and SiC substrates is shown. The high-performance GET-SBD with L_{AC} of 5 μm demonstrates a power FOM ($BV^2/R_{ON,SP}$) as high as 2.5 GW/cm^2. However, GET-SBD with L_{AC} of 10 μm did not show further increase of BV due to the limitation from the buffer.

3.3 Evaluation of Power Diodes

In order to deliver high power in Si or SiC power diodes, large areas are needed due to the vertical current flow mechanism. For the lateral AlGaN/GaN SBDs and

HEMTs, the on-state and off-state currents scale with the anode finger width. To allow high forward currents in lateral AlGaN/GaN diodes, the total anode width should be widened. In principle, the on- and off-state currents scale linearly with the anode width. In Figure 3.16(a), the top view of GET-SBD power diode is shown. The width of single anode finger is 1 mm, and there are 10 GET-SBDs in one power diode fabricated in an interdigitated fashion. Thus the total anode width of this multi-finger power diode is 10 mm. Figure 3.16(b) illustrates that the designed power diode consists of 10 single finger GET-SBDs in parallel. A top view of a single anode finger GET-SBD is shown in Figure 3.16(c) with some diode layout parameters. According to the on-state characteristics of small diodes in Figure 3.13(b), the scaled-up power diode should, in principle, deliver ∼4 A at 2 V at 25 °C.

Multi-finger GET-SBD power diodes with 10-mm anode width have been characterized with the substrate grounded. The breakdown characteristics of GET-SBD1 and GET-SBD2 at 25 °C are shown in Figure 3.17(a). The statistical leakage values (at V_R of −200 V) at 25 °C and 150 °C for GET-SBD1 and GET-SBD2 power diodes on 200-mm silicon substrates are presented in Figure 3.17(b) and (c), respectively. These results show a good yield of the power diodes, and the optimized GET-SBD demonstrates a leakage current of 1.3 μA at 25 °C and 3.8 μA at 150 °C with very weak temperature-dependence. This indicates that the optimized GET-SBDs with IMP TiN anode metal are promising for high-temperature and high power applications where a low leakage current is required.

In Table 3.3, a comparison of the temperature dependent leakage (at −200 V) of Si, SiC and GaN power diodes is shown. The forward voltage to deliver 1 A for three diodes is around 1.2 V (not shown in the table). The SiC diode shows the lowest leakage at both 25 °C and 150 °C. A clear advantage of the GaN diode (GET-SBD2) compared with Si diode lies in its weak temperature dependent leakage. This allows for the high temperature applications based on the GaN technology. Our Au-free GET-SBD power diode with low leakage and high forward currents demonstrates to be a promising candidate for low cost and high-performance power electronics.

In Figure 3.18 (a) and (b), the statistical forward characteristics (at 25 °C and 150 °C) of 25 power diodes with 10-mm anode width are presented for the GET-SBD1 and GET-SBD2 architectures. The forward current reduction at 150 °C is due to the mobility degradation of the 2DEG and an increased sheet resistance [77]. A high forward current of ∼4 A (at 2 V) at 25 °C for both GET-SBD1 and GET-SBD2 power diodes is demonstrated, together with a low leakage current shown in Figure 3.17. By comparing the results with those of small diodes in Figure 3.8, the on-state currents scale very well with the perimeter (i.e. the anode width). This statistical evaluation confirms that the GET-SBD architecture with IMP TiN as the Au-free anode metal shows excellent performance with low leakage and high forward currents which has been demonstrated on 10-mm power diodes with high yield and good uniformity over a 200-mm silicon wafer.

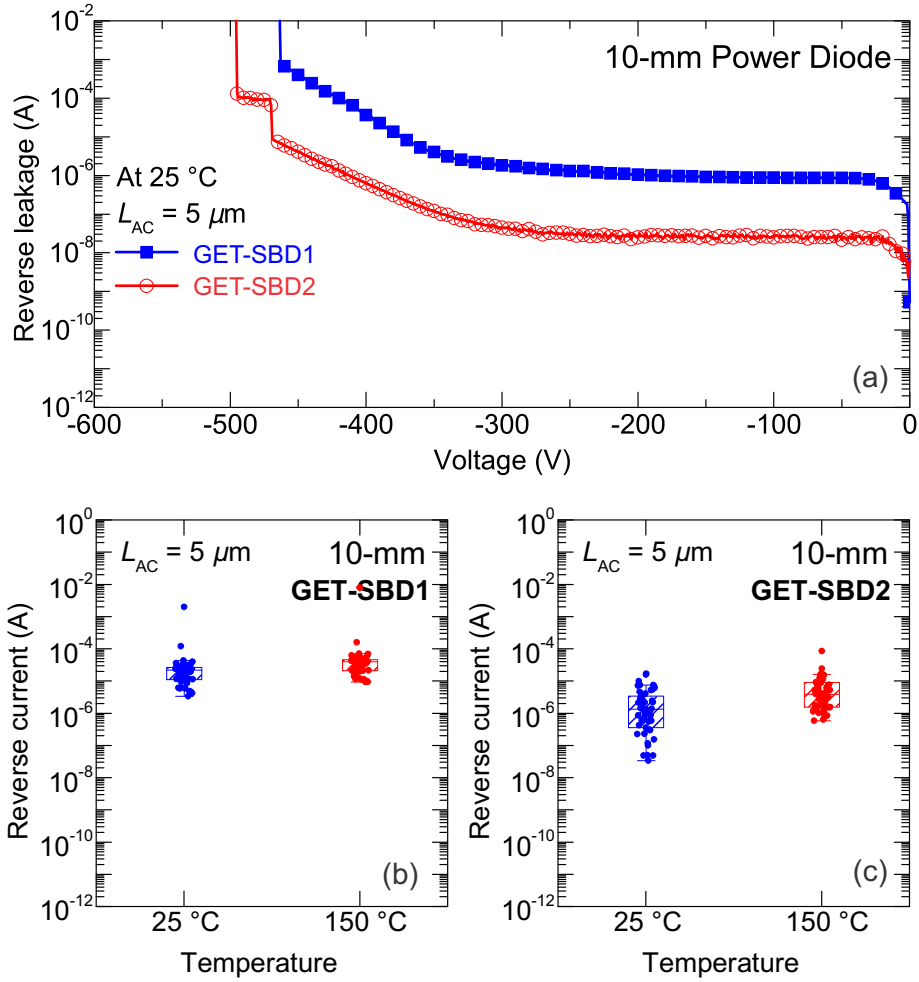


Figure 3.17: (a) Typical off-state characteristics of GET-SBD1 and GET-SBD2 power diodes measured at 25 °C. (b) The statistical leakage values of GET-SBD1 and GET-SBD2 (at 25 °C and at 150 °C) are shown in (b) and (c), respectively.

3.4 Summary and Conclusions

In this chapter, further performance optimization was presented on AlGaN/GaN SBDs with gated edge termination. Firstly, a carbon-doped AlGaN buffer was selected due to its lower buffer leakage and higher buffer breakdown voltage than those of a UID buffer. With this carbon-doped buffer, the AlGaN/GaN GET-SBDs showed promising

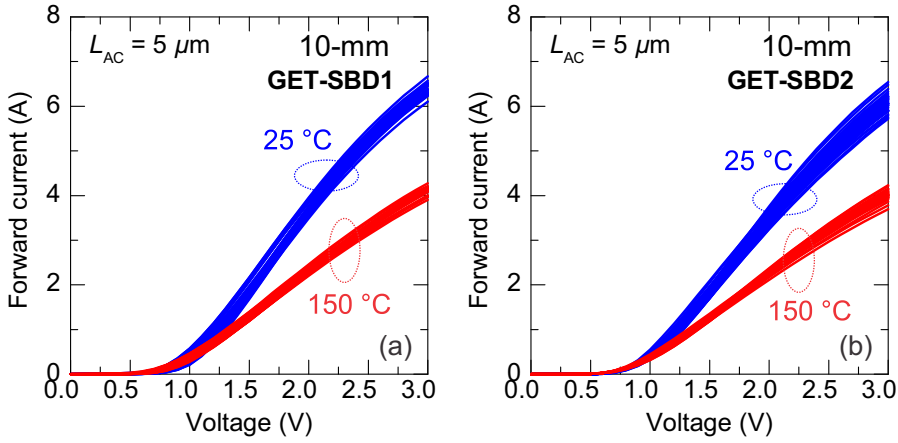


Figure 3.18: The forward characteristics of GET-SBD1 power diodes (a) and GET-SBD2 power diodes (b) measured at 25 °C and 150 °C. The results show high yield and good uniformity over 200-mm silicon wafers.

Table 3.3: Temperature Dependent Leakage (at V_{AC} of −200 V) Benchmarking of Si, SiC, and Lateral GaN Power Diodes

Device	I_{OFF} (25 °C)	I_{OFF} (150 °C)	I_{OFF} (150 °C)/I_{OFF} (25 °C)
GaN Diode	1.3	3.8	2.9
Si Diode (1N4935)	0.1	200	2000
SiC Diode ([78])	0.01	0.1	10

reverse characteristics for 200-V applications.

The gated edge termination was applied in the AlGaN/GaN SBDs to enable a redistribution of the off-state electric field and a suppression of the leakage current. A further leakage reduction was demonstrated by optimizing the TiN anode metal. The GET-SBDs with IMP TiN showed stronger blocking capability of the leakage than diodes with standard PVD TiN attributing to a higher metal work-function in the IMP TiN. It was also shown that the leakage level is independent of the anode-to-cathode spacing L_{AC} and L_G, this indicates that the edge termination effectively pinches off the 2DEG channel and increases the overall blocking barrier. A lower leakage current was realized in the GET-SBD with the high-ϕ_m IMP TiN due to a smaller tunneling probability, this has been interpreted from the point of view of the band diagram.

The GET-SBD1 and GET-SBD2 both showed high forward currents at 25 °C and 150 °C. Forward modeling showed that a dislocation-assisted tunneling mechanism can

be the dominant process for non-recessed SBDs. With AlGaN barrier recessing, direct tunneling and other tunneling mechanisms can be additional processes improving the forward characteristics. To further improve the on-state performance, the scaling down of the L_G parameter proved to be an effective method without degrading the reverse characteristics. This leads to a reduction of the forward voltage and a more compact device design. This work demonstrates that lateral AlGaN/GaN SBDs with a record performance in terms of low leakage and low forward voltage have been realized in the GET-SBDs in a Au-free technology.

Finally, excellent characteristics have been demonstrated on large power diodes with good yield and uniformity (at both 25 °C and 150 °C) on 200-mm silicon substrates and realized by fabrication in a CMOS-compatible process line.

Chapter 4

Dynamic Stability of GaN Diodes

In this chapter, we discuss the motivation and measurement procedure to assess the dynamic characteristics of GaN diodes. Pulsed current–voltage and current-based transient measurements are developed to evaluate the trapping/de-trapping mechanisms when the diode is subject to off-state stress. Dominant surface trapping is observed, and an improvement is experimentally realized by using cleaning steps and a better passivation layer, and improved dielectric materials.

4.1 Introduction

In DC–DC power converters, the average output voltage is controlled by modulating the on and off durations (t_{ON} and t_{OFF}) of the active switch (i.e. power transistor). This method is called "pulse–width modulation" (PWM) switching, and the switch duty ratio D (i.e. $t_{ON}/(t_{ON} + t_{OFF})$) is varied at a constant frequency.

Power converters based on GaN technology are promising due to its high-frequency capabilities, thus passive components (inductors, capacitors) can be miniaturized leading to more compact and energy-efficient power systems. Due to the high sheet density and mobility of the 2-dimensional electron gas at the AlGaN/GaN interface, GaN HEMT as a uni-polar device can operate at a frequencies above MHz compared with the typical low frequency ($\sim$ 100 kHz) capability of a CoolMOS which is mainly due to the switching losses. GaN-based electronic devices as unipolar devices not only can be operated at much higher frequencies, but also they allow fast turn-on and turn-off of the device with much narrower pulses ($<$ 100 ns), opening possible applications which are unreachable for conventional silicon-based devices.

However, the dynamic stability of GaN devices can be affected by the existence of "intrinsic" and "extrinsic" traps in the epi-stack that has been reported in GaN RF and Power Transistors. A short stress pulse (in on-state and off-state) can result in electron filling of traps, and the characteristic time of the de-trapping mechanism normally is much longer than the switching period. The trapped electrons basically deplete the 2DEG due to the charge balance, resulting in an increased R_{ON}. This pre-bias dependent on-resistance of the GaN devices is typically regarded as dynamic R_{ON}. Thus, a current-reduction or in some cases even a total current collapse phenomenon have been observed.

In this chapter, a pulsed current-voltage measurement to assess the dynamic characteristics of GaN diodes is presented. A N_2 plasma cleaning step was developed to

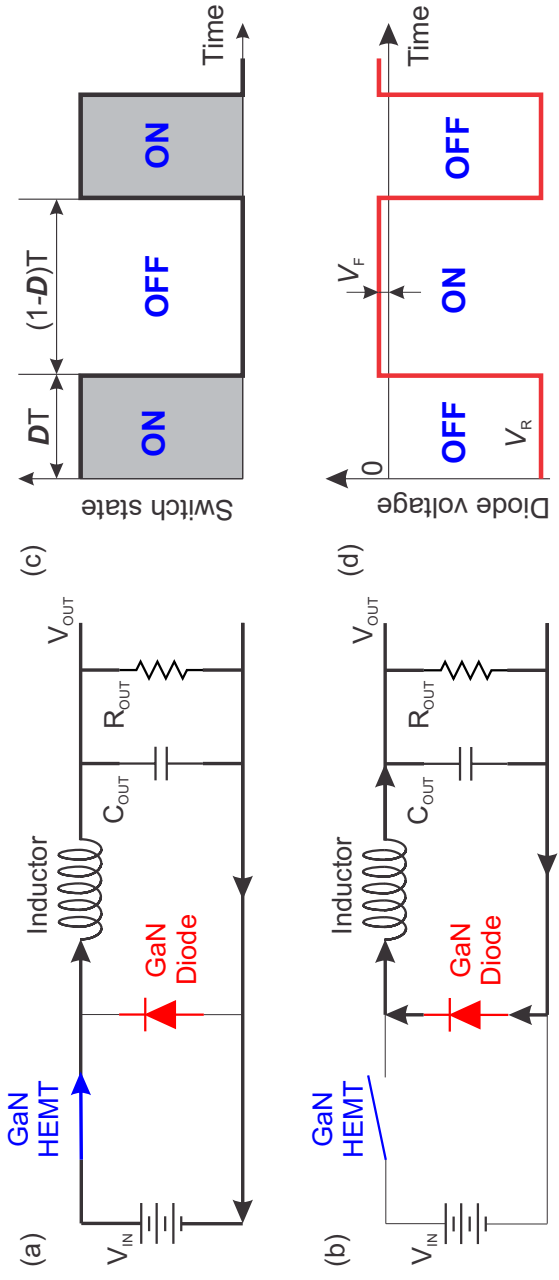


Figure 4.1: The circuit configuration of a buck converter based on GaN technology when the GaN HEMT is in on-state (a) and off-state (b), respectively. (c) The switching state of the transistor which is controlled by a gate driver. (d) The switching of the voltage across the GaN diode in response to the switching state of the GaN transistor.

significantly improve the dynamic stability of the GaN diodes. To further understand the trapping/de-trapping mechanisms in GaN diodes under off-state stress, a combined stress and current-based transient measurement is proposed to study the current-reduction and current collapse phenomena in GaN diodes. Finally, a TCAD-based model was used to understand the total current collapse phenomenon in GaN conventional SBDs and GET-SBDs.

4.2 Pulsed current–voltage characterization

This section will show the motivation of the dynamic characterization on GaN diodes based on the circuit analysis of a buck converter as an example. A pulsed measurement procedure will be proposed to study the pulsed current-voltage (I–V) characteristics of GaN diodes.

4.2.1 Motivation of Dynamic Characterization

GaN diodes, as a passive switching component, do not have an additional terminal as a transistor to control the switching. Typically a diode in a switching circuit is used to regulate the current flow and switch in a passive fashion. In Figure 4.1(a) and (b), the current flow in a GaN-based buck converter is shown when the GaN HEMT is in on- and off-state, respectively. As an active switch, the switching of the GaN HEMT is controlled by the gate terminal through a gate driver. In Figure 4.1(c) and (d), the switching state of the GaN HEMT and the voltage across the GaN diode are shown for the respective switching states.

A buck converter is a typical DC/DC voltage convertor stepping down a high input voltage to a low output voltage. When the GaN HEMT is biased in the on-state, the voltage drop across the 2DEG channel is negligible and the diode is operating in the reverse. When the GaN diode is biased in the off-state ($V_R \approx -V_{IN}$), only a small leakage current will flow through the GaN diode. Thus, a net positive voltage is induced across the inductor when the current in the circuit is linearly increasing. In this state, the inductor is charged with stored magnetic energy. When the GaN HEMT is turned off, the inductor is discharging its stored energy to keep the current flowing through the load. In this state, the diode is forced to turn on with a small forward voltage across the diode. The forward voltage is designed to be small to minimize the on-state static power loss. As can be seen in Figure 4.1(d), the GaN diode is switched passively from OFF to ON when the GaN HEMT is switched actively from ON to OFF.

When the GaN HEMT and diode are operating in off-state, a high electric field is present in the vicinity of the gate or anode edge. The electrons can be injected from the anode contact into trap states at the AlGaN surface or in the GaN/AlGaN epi-layers, reducing the 2DEG density in the channel and degrading the electrical characteristics of the device. As an example to illustrate this trapping effect, the current reduction phenomena in GaN HEMT and SBD are shown in Figure 4.2(a) and (b), respectively. After the GaN HEMT and SBD are subject to a pre-bias in off-state, a typical lower on-state current is observed at fixed V_{DS} or V_F. In the case of GaN SBD, it can also be interpreted that a higher V_F is needed for the degraded device to allow a fixed on-state

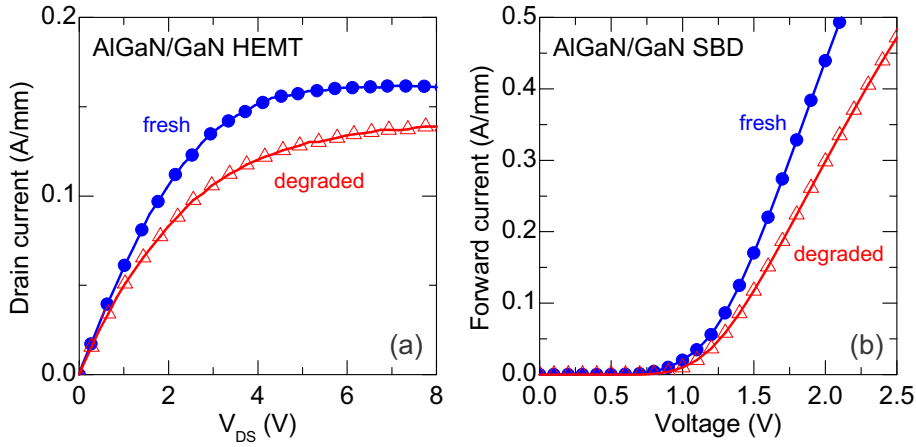


Figure 4.2: The illustration of current degradation phenomena in AlGaN/GaN HEMT (a) and in AlGaN/GaN SBD (b) when HEMT and SBD are subject to an off-state pre-bias stress pulse.

current to pass through the diode. This leads to an increase of the static power loss. Therefore, it is essential to design a GaN diode with low and stable forward voltage.

4.2.2 Measurement Procedure

To examine the dynamic behavior of AlGaN/GaN SBDs, a measurement procedure is developed and shown in Figure 4.3. An Agilent B1505A Semiconductor Device Analyzer is used as the pulse generator to measure the pulsed *I*–*V* characteristic. Each point of the forward *I*–*V* characteristics is preceded by a 10-ms stressing pulse (quiescent state) at a negative bias (V_R), as is shown in Figure 4.3(b). The rise time from the stressing voltage to the forward voltage is ∼2 ms. Though the stressing and rising times are long compared to the real operation of the device, this measurement technique provides a fast feedback on the dynamic stability of the diode, moreover a cumulative stress can build up over multiple cycles of the switching circuit. This longer term reliability issue can be captured by this technique using long stressing pulses.

During the filling pulse, the high electric field assists the electron injection to the trap states at various locations. The forward characteristics are then affected by the trapping phenomena occurring during the filling pulse, an example is illustrated in Figure 4.3(c). Depending on the trapping location, the turn-on voltage or the on-resistance, or combined effects of increased turn-on voltage and on-resistance can occur and result in the degradation of the forward voltage. The stressing pulse V_R can be varied to investigate the bias-dependent trapping mechanisms. As is shown in Figure 4.3(c), a full forward characteristic of the diode can be visualized due to a linear increasing positive pulse after the pre-bias stress state. Bias-dependent pulsed *I*–

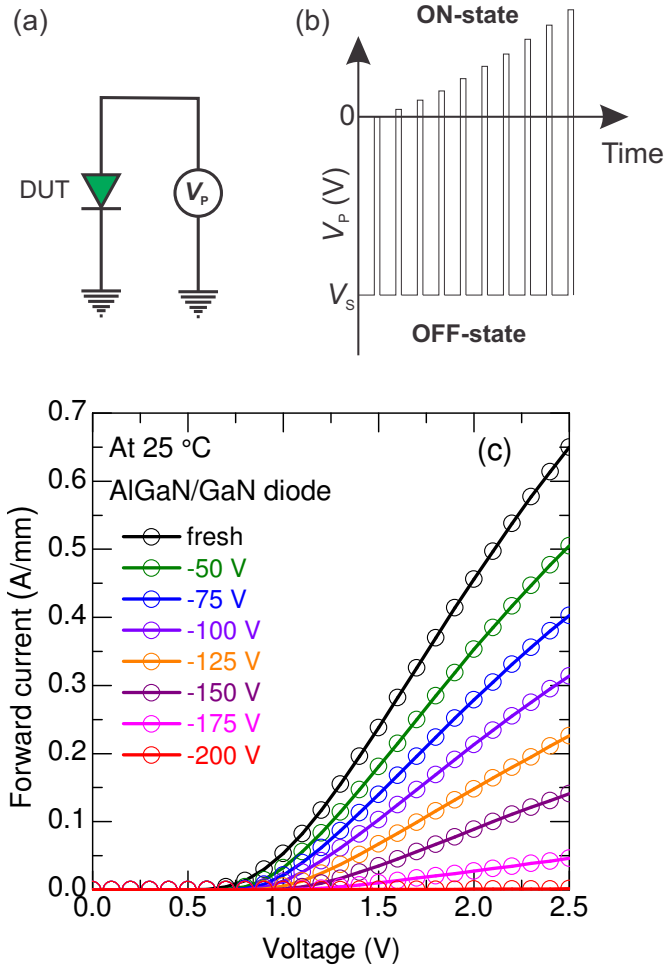


Figure 4.3: (a) Experimental set-up for pulsed *I*–*V* measurement on AlGaN/GaN SBD. (b) Measurement technique: forward current was measured with a pulsed positive voltage V_F when a constant stressing voltage V_R was applied on the Anode with stressing time period t_S of 10 ms. (c) An example of pulsed *I*–*V* characteristics of AlGaN/GaN diode showing pronounced dynamic R_{ON} increase.

V characteristics are shown in Figure 4.3(c) as an example; a gradual current reduction is observed and finally brings about total current collapse due to severe trapping after a pre-bias at −200 V. The full forward characteristic can give a clear indication of the dominant trapping mechanism. For instance, a severe R_{ON} degradation without increase of the turn-on voltage can point to dominant trapping in the access region[1] instead of the trapping at the anode edge. Otherwise, the Schottky barrier height would be increased. The challenge is that a mixed trapping location and several trap levels (with different activation energies) is typically involved during the stress state. In this chapter and chapter 5, we will analyze dominant surface trapping and bulk buffer trapping, respectively.

4.3 Dominant Surface Trapping

In this section, the impact of AlGaN surface (below the Schottky contact) cleaning on the dynamic characteristics of GaN SBDs and GET-SBDs is studied. It will be demonstrated that the current degradation (measured in pulsed regime) can be reduced by introducing a N_2 plasma cleaning step in the anode metal deposition chamber. The cleaned GET-SBD, with lower electric field at the anode edge compared with conventional AlGaN/GaN SBD, shows a more stable dynamic R_{ON}.

4.3.1 Experimental Details

On top of 200 mm (111) Si wafers, the following epitaxial layers were grown by Metal Organic Chemical Vapor Deposition (MOCVD): 200 nm AlN nucleation layer (on top of the Si substrate), followed by a 2600 nm-thick AlGaN-based buffer, 150 nm-thick GaN channel and 10 nm-thick $Al_{0.25}Ga_{0.75}N$ barrier. The epitaxial stack was passivated with a 140 nm-thick Si_3N_4, grown by Rapid Thermal Chemical Vapor Deposition (RTCVD). Then, the GET anode was fabricated. After opening the anode region in the Si_3N_4 surface passivation, a 15 nm-thick RTCVD Si_3N_4 was deposited at 650 °C and annealed at 700 °C. The Si_3N_4 edge termination was etched open by SF_6 dry etching to define the Schottky contact. Then, two types of cleaning steps were tested [79]:

- No cleaning, as a reference. In this condition, a mono-layer (∼0.2 nm) oxide was found at the exposed surface (*courtesy: ir B. De Jaeger, D. van Dorp, imec*).
- Wet cleaning with HCl (10 min, 18 wt%) and TMAH (10 min, 65 °C), followed by *in-situ* N_2-based plasma cleaning inside the anode metal sputtering tool (i.e. without air break before the metal deposition). The N_2 plasma conditions were 100 W RF power, 50 W bias power and 36 sccm N_2 flow (*thanks to Dr. S. Lenci and Dr. M. Van Hove for the development of this cleaning step*).

The anode metal, subsequently deposited and patterned, consists of a 20 nm TiN/ 20 nm Ti/ 250nm Al/ 20 nm Ti/ 60 nm TiN Au-free stack. The processing continued with the Au-free cathodes (a Ti/Al/Ti/TiN-based stack, annealed at 550 °C) and Au-free backend fabrication. During the plasma cleaning treatment, the AlGaN surface of

[1] Access region, for AlGaN/GaN diode, is the region between anode and cathode contacts.

the conventional SBD is cleaned as well. A schematic illustrating the AlGaN surface cleaning on conventional AlGaN/GaN SBD and GET-SBD is shown in Figure 4.4(d).

4.3.2 Electrical Results and Discussions

4.3.2.1 Pulsed *I–V* Characteristics

In Figure 4.4(a) and (b), bias-dependent pulsed *I–V* characteristics of the GET-SBD for non-cleaned and cleaned conditioins are shown, respectively. A significant improvement of the forward characteristics is achieved with this critical cleaning step. After a pre-bias at −150 V, the forward voltage (at forward current of 100 mA/mm) of the non-cleaned GET-SBD becomes 1.56 times of the fresh device comparing with 1.06 for the cleaned GET-SBD. After the GaN diode turns on, the series resistance (R_{ON}) takes up the additional voltage applied, resulting in ideally linear *I–V* characteristics. In Figure 4.4(c), the normalized R_{ON} (referred to the value of fresh diodes) of SBD and GET-SBD for two cleaning conditions as a function of the stress pulse voltage is summarized. Without surface cleaning, it shows that the conventional SBD and GET-SBD are almost identical in terms of this dynamic R_{ON} increase. Though a lower surface electric field was achieved in GET-SBD, no significant improvement in the dynamic R_{ON} is achieved. This indicates that the surface traps can be charged up at relatively low stress voltage, affecting the dynamic R_{ON}. After the removal of the surface trap by plasma cleaning, both SBD and GET-SBD show significant improvement in dynamic R_{ON} stability. Furthermore, the GET-SBD shows better stability compared with SBD. This is reflected in the fact that the residual dynamic R_{ON} increase and trapping effects are more dependent on the electric field. It is more likely that this residual trapping mechanism is due to the electron injection at the AlGaN barrier/Si_3N_4 interface or electron injection into the Si_3N_4 layer.

Figure 4.4(d) presents the surface plasma cleaning procedure [2]. Due to the exposed AlGaN surface to air, a mono-layer of oxide (∼0.2 nm) was formed at the AlGaN surface (*courtesy: ir. B. De Jaeger, imec*). In the fresh condition, the impact of this mono-layer on the forward characteristic is negligible due its thin nature. It is possible that some traps are located at the oxide/AlGaN interface. After a pre-bias stress pulse, these traps at the oxide/AlGaN interface can be filled resulting in the forward current degradation. With the plasma N_2treatment, it is most likely that the mono-layer oxide was removed and some dangling bonds (i.e. V_N) were repaired. J.H. Kim *et al.* showed that nitride-based plasma pre-treatment prior to the SiN_x passivation reduces the dynamic R_{ON} phenomenon of the GaN HEMT [80]. In our GaN SBD and GET-SBD, the interface between AlGaN and Si_3N_4 was not cleaned. It was reported that the nitride-biased plasma can remove certain traps and recover nitrogen-vacancy (V_N)-related defects. It is possible that the residual dynamic R_{ON} increase of SBD and GET-SBD is due to the electron filling of traps located at the AlGaN/SiN interface.

Another important point worthy of notice is that the series resistance dominated region of non-cleaned GET-SBD is not perfectly linear (in Figure 4.4(a)). For instance, the

[2] It is believed that the plasma cleaning only removed the mono-layer oxide without recessing the AlGaN barrier. From HRTEM image, we did not observe significant changes of the AlGaN barrier after the plasma cleaning step (*courtesy: ir. B. De. Jaeger*).

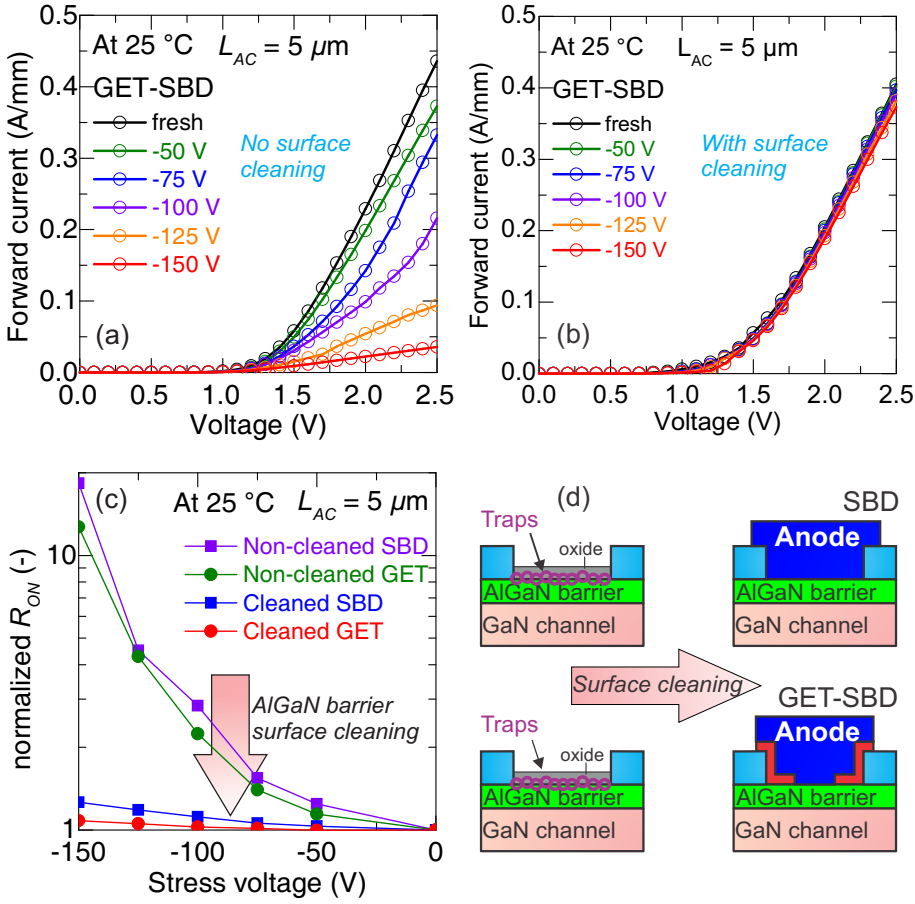


Figure 4.4: Pulsed *I–V* characteristics of AlGaN/GaN GET-SBD with (a) and without (b) surface cleaning steps. (c) The comparison of normalized R_{ON} for SBD and GET-SBD under two cleaning conditions. (d) The schematic illustration of the surface cleaning in SBD and GET-SBD architectures.

slope of the linear I–V characteristics (for the case of V_R at −100 V) changes with the on-state voltages. This is due to the de-trapping of the surface states triggered by the positive voltage applied at the anode. Since the trap states are located below the anode metal, the positive potential attracts the electron and assists the de-trapping process. Once some of surface states are de-trapped, the R_{ON} becomes relatively lower resulting in a sudden change of the slope. Based on this observation, we will design current transient measurements trying to avoid applying positive voltage at the anode. Detailed description of the measurement procedure will be discussed in the following section.

4.3.2.2 Constant Voltage Stress

To further understand the R_{ON} increase of SBD and GET-SBD with plasma cleaning, constant voltage (V_R at −100 V) off-state stress measurements were carried out on Agilent HP4156C. The DC characteristics of cleaned SBDs and GET-SBDs (from −20 to 3 V) were measured after certain stressing time intervals T_S (10, 1010, 3010, 6010, 10010, and 15010 s).

In Figure 4.5(a) and (b), the DC characteristics of SBD and GET-SBD (fresh and stressed device) are shown, respectively. Both devices show 1–2 orders of magnitude reduction in leakage current without severe on-state degradation. This confirms that there is still residual trapping in the vicinity of the Schottky contact affecting the barrier height, thus leakage reduction is observed due to electron-electron Coulomb repulsion.

By using the equation describing the thermionic emission model, the apparent barrier height and ideality factor can be extracted on the fresh and stressed diodes. The ON-resistance is extracted from the linear region. The results are summarized below in Table 4.1 for both SBD and GET-SBD architectures. It can be observed that the leakage current reduction in stressed SBD and GET-SBD is related to an increase of the apparent barrier height. An electron trapping occurs at the anode edge, increasing the energy barrier height and reducing the tunneling probability of the leakage. The apparent barrier height might be lower than the real value, as the ideality factor deviates severely from unity due to other current transport mechanisms. However, the increase of the barrier height after off-state stressing can qualitatively reflect the trapping effects on the leakage. Additionally, the area with trapped electrons can act as a virtual gate and deplete the 2DEG, increasing the on-resistance. This increase of R_{ON} was also shown on the stressed SBD and GET-SBD in Table 4.1.

4.4 Current Transient Measurements

This section presents a current-based transient methodology for the trap analysis on AlGaN/GaN SBDs. The trap energy level and cross-section of different traps can be evaluated from this thermally stimulated transient spectroscopy. Furthermore, the physical location of different trapping mechanisms can be indicated by the leakage behavior of the diode during the transient measurement.

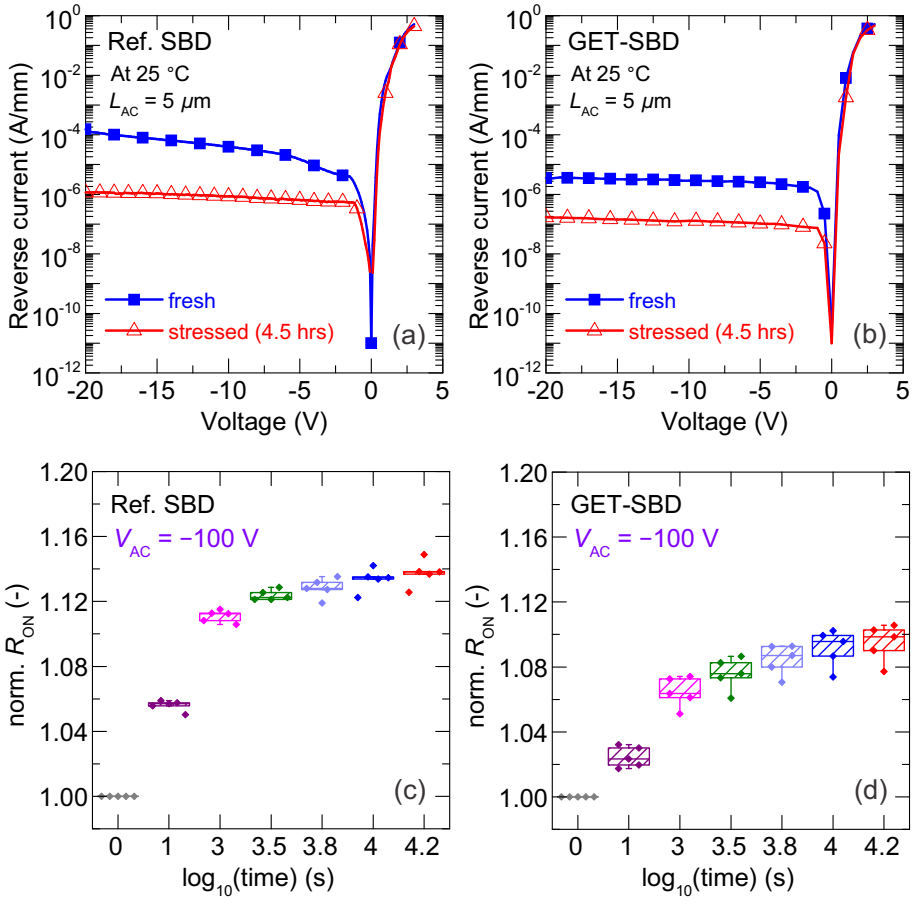


Figure 4.5: (a) *I–V* characteristics of conventional AlGaN/GaN SBD with cleaning step at fresh and after stressing at −100 V for 4.5 hours. (b) *I–V* characteristics of AlGaN/GaN GET-SBD with cleaning step at fresh and after stressing at −100 V for 4.5 hours. The statistical normalized R_{ON} of SBD (c) and GET-SBD (d) as a function of the stressing times up to 4.5 hours.

Table 4.1: The leakage current, extracted barrier height, ideality factor, and on-resistance of fresh and stressed SBD and GET-SBD.

Device	Leakage at −20 V (A/mm)	ϕ_B (eV)	ideality factor n (-)	On-resistance Ω × mm
fresh SBD	1.5×10^{-4}	0.66	1.57	2.19
stressed SBD	1.2×10^{-6}	0.69	1.31	2.73
fresh GET	3.5×10^{-6}	0.56	2.12	2.48
stressed GET	1.7×10^{-7}	0.62	1.95	2.67

4.4.1 Methodology

Several researchers have performed the study of trapping effects in AlGaN/GaN transistors by combined pulsed and R_{ON} transient measurements. Joh *et al.* have presented a current-transient methodology to study the electron trapping in GaN HEMTs [81]. Meneghini *et al.* have investigated the trapping mechanisms in GaN HEMTs by investigating the role of bias conditions [82]. Liao *et al.* and Bisi *et al.* have reported the back-side virtual gate effects in AlGaN/GaN HEMTs due to the electron trapping in the AlGaN back-barrier [83, 84].

To identify the related traps (activation energy, cross-section and physical location) affecting the diode electrical characteristics after stressing, we used a current transient methodology which consists of an off-state stress stage and a current recovery stage shown in Figure 4.6(a). The measurements were performed by using a Semiconductor Device Analyzer (Agilent B1500A). During the stress, the device was biased in the off-state for 10 s to fill the traps. The stress voltage (−100 V) was applied at the Anode, and Cathode1 and Cathode2 were grounded. During the recovery, the Anode and Cathode1 contacts were grounded while 0.5 V was applied on the Cathode2. After the removal of the stress voltage at the Anode, the 2DEG channel will be replenished partially. In the recovery stage, we will monitor the recovery of the resistive current through the 2DEG resistor instead of the diode forward current (in the on-state). It needs to be noted that the voltage between Anode and Cathode2 is −0.5 V, in this case there is a leakage current flow through the Anode at its perimeter [35]. Whenever there is a de-trapping of electrons at the AlGaN surface, the effective barrier height ϕ_B will reduce and the diode leakage current will show an increase accordingly. The Anode contact effectively acts as a potential sensor during the de-trapping stage. The recovery measurements were carried out at temperatures ranging from 25 °C to 135 °C with a predefined recovery time of 3333 s. The recovery current (through Cathode2) and the diode leakage current (at $V_R = -0.5$ V) are shown in Figure 4.6(b). The 2DEG resistive current is more than three orders of magnitude higher than the leakage current, and the resistive current is used for the extrapolation of traps.

To extract the activation energy of traps, the transient data were firstly fitted by a least-mean-square approach with a sum of 400 exponentials and equally spaced time constants logarithmically ranging from 0.01 s to 10000 s [81]. The fitting equation in

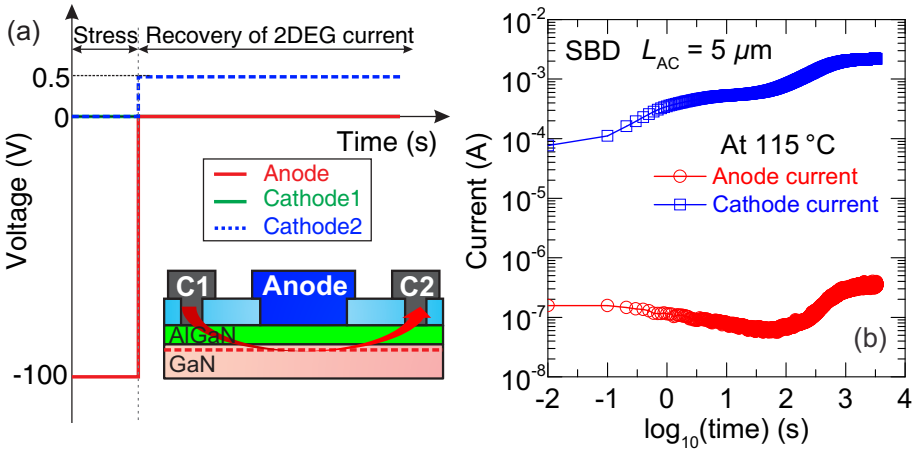


Figure 4.6: (a) The current transient measurement methodology developed in this study. The device is biased in the off-state (V_R = −100 V) for 10 s before the recovery of the 2DEG resistor. (b) The current is monitored through Cathode2 and Anode during the recovery. The recovery of the 2DEG resistor (through Cathode2) will be used for the trap analysis, and the current through the Anode is the diode leakage current at V_R = −0.5 V.

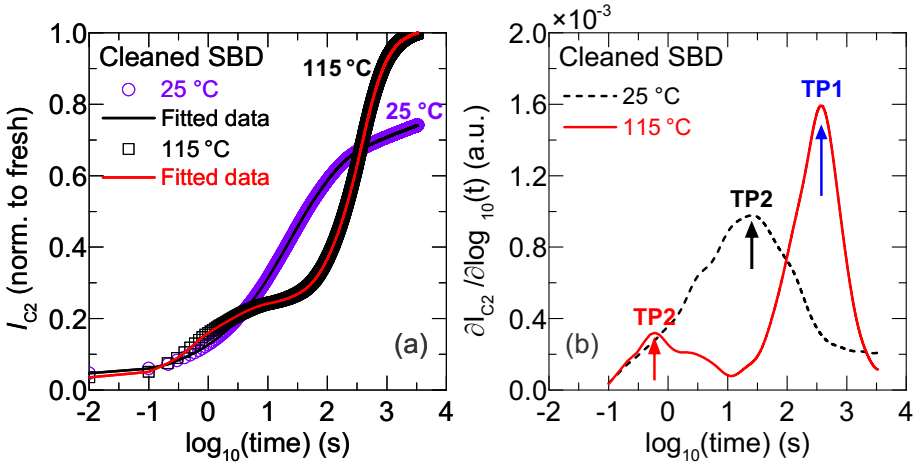


Figure 4.7: (a) The normalized recovery current measurement at 25 °C and 115 °C. (b) The time-constant spectra (derivative of the current transients) evaluated at 25 °C and 115 °C.

this approach can be expressed as:

$$I_{C2} = \sum_{i=1}^{400} a_i \exp\left(-t/\tau_i\right) + I_0. \tag{4.1}$$

The underlying assumption of this method is that a current transient involves independent de-trapping processes with a characteristic detrapping time-constant in an exponential way [81, 85]. The fitting algorithm used is to minimize the sum of $|I_{C2} - I_{\text{data}}|^2$ in the least-mean-square approach, so that the fitted curve closely represents the measurement data. The data from the fitting curve can be used to take derivatives to generate the time-constant spectra. In Figure 4.7(a), the raw data and fitted curve of the recovery currents at 25 °C and 115 °C are displayed, showing a perfect overlay. The current has been normalized to the value obtained from the fresh device at 25 °C and 115 °C, respectively. In this way, the thermal effect on R_{ON} is excluded. At room temperature, the device has recovered 74.13 % after recovery time of 3333 s. To have a full recovery of the device, it will need much longer time than 3333 s at 25 °C, which means that this de-trapping process is very slow. It is expected to have faster detrapping kinetics at higher temperatures (i.e. at 115 °C) with predefined recovery time, which is shown in Figure 4.7(b). By taking the derivatives of the current transients, the time-constant spectra can be shown in Figure 4.7(b). At 115 °C, two distinct time constants were observed, which are labeled at TP1 ($\tau \sim 373.6$ s) and TP2 ($\tau \sim 0.6$ s). At room temperature, there is only one time constant ($\tau \sim 25.7$ s) shown which corresponds to the de-trapping of TP2. It also indicates that the diode is not fully recovered as the recovery mechanism related to TP1 falls outside of the measured time window. Since TP2 detraps faster than TP1, it means that TP1 features a deeper state with longer detrapping characteristic time. The activation energy of TP1 and TP2 can be extracted by performing the transient measurements at various temperatures and plotting the Arrhenius graph.

4.4.2 Electrical Results and Discussions

To enable the extraction of the trap information (activation energy, cross-section), temperature-dependent transient measurements (from 65 °C to 135 °C) have been carried out. The time-constant spectra (derivative of the transients) for de-trapping transient of TP1 and TP2 are shown in Figure 4.8(a) evaluated from 65 °C to 135 °C where the detrapping time-constants of both TP1 and TP2 appear in this time window. With these temperature-dependent measurements, the activation energy and cross-section of TP1 and TP2 can be extrapolated based on the equation(4.2) below [86]:

$$\ln\left(\tau_n \times T^2\right) = \left(E_C - E_T\right)\frac{1}{kT} - \ln\left(\sigma_n \times \gamma_n\right), \tag{4.2}$$

where σ_n, E_T, and γ_n are the capture cross-section, trap level, and $\gamma_n = 3.25 \times 10^{21}(m_n/m_0)$ $\text{cm}^{-1}\text{s}^{-1}\text{K}^{-2}$ [86]. In the formula for γ_n, m_n is the electron density-of-states effective mass [87]. We used a value of $\gamma_n = 6.5\times\ 10^{20}$ $\text{cm}^{-1}\text{s}^{-1}\text{K}^{-2}$ for the

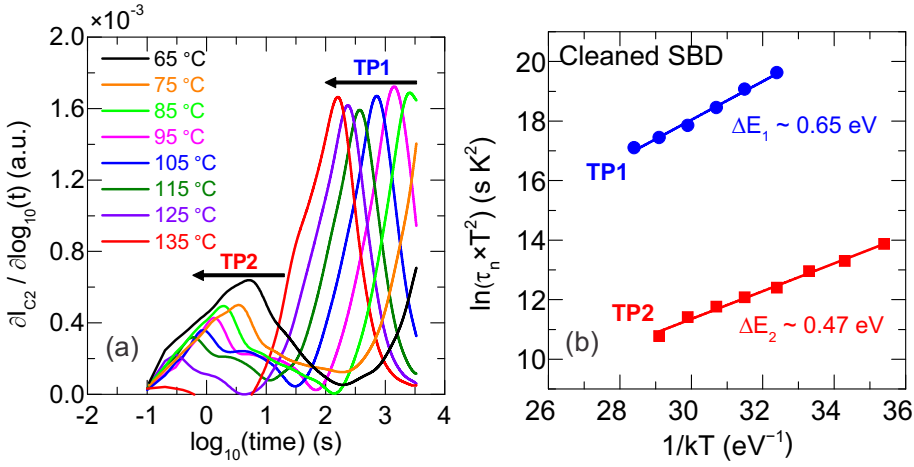


Figure 4.8: (a) The time-constant spectra (derivative of the current transients) evaluated from 65 °C to 135 °C showing the de-trapping kinetics of TP1 and TP2. (b) Arrhenius plot of the time constant spectra for TP1 and TP2.

extraction of the capture cross-section. The Arrhenius plot (shown in Figure 4.8(b)) indicates that TP1 has an activation energy of 0.65 eV and a cross-section of 0.89×10^{-20} cm^{-2}, while TP2 has an activation energy of 0.47 eV and a cross-section of 2.85×10^{-20} cm^{-2}.

The small apparent cross-section can be explained by Hermann and Warfield's model [88, 89], in which the cross-section decreases exponentially with the depth:

$$\sigma_n(E,x) = \sigma_n(x) = \sigma_n(0)\exp(-x/\lambda) \tag{4.3}$$

where λ is the tunneling attenuation constant. This model has been proposed to study the Si/SiO_2 interface states by using the charge pumping technique. It is possible that the de-trapping mechanism of the trap states involves additional transport process.

To identify the physical location of these two trapping/de-trapping defects, we have analyzed the leakage current through the Anode during the recovery transient, as is shown in Figure 4.9. The leakage current comes from the injection of electrons from the anode into the GaN channel, and it is exponentially dependent on the SBH ϕ_B. In the inset group of Figure 4.9, it shows the leakage reduction and barrier height increase during stress and electron trapping. And the leakage in Figure 4.9 actually reflects the barrier height variation during the detrapping processes. With the de-trapped electrons at the AlGaN barrier surface in the vicinity of the Schottky contact, the SBH reduces resulting in an increase of the leakage current. By comparing Figure 4.9 with Figure 4.8(a), the time period of the leakage increase (from 95 °C to 135 °C) matches

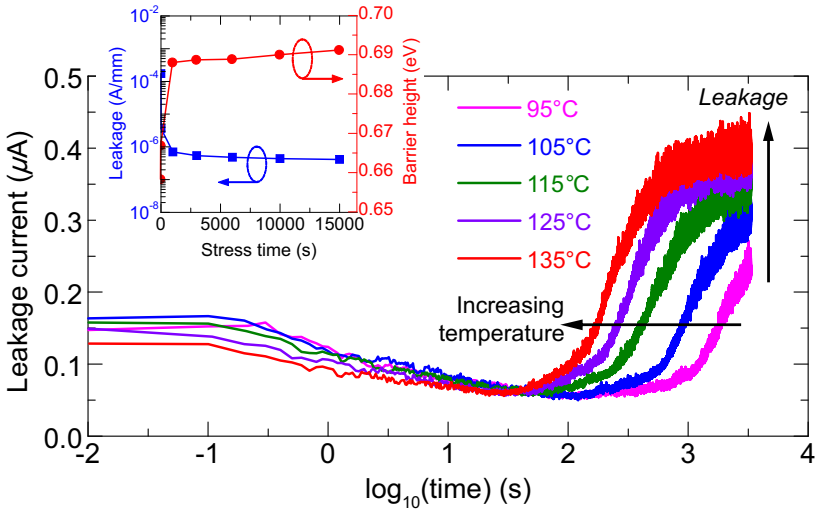


Figure 4.9: The SBD leakage during the recovery monitored from 95 °C to 135 °C.

well with the de-trapping time constants of TP1 at various temperatures. During the de-trapping of the TP2, the leakage current shows a slight reduction rather than increase, this may be due to the reduction of voltage drop across the diode during the de-trapping of the states in the GaN channel.

The electron trapping of both TP1 and TP2 will contribute to the R_{ON} increase as shown in Figure 4.5(c), however, only the electron trapping of TP1 located at the surface results in the leakage reduction and barrier height ϕ_B increase. For the trap states far away from the anode contact, they can be charged in the off-state stressing period due to the vertical and lateral depletion region and the electric field penetration in it. However, they should be ideally not affecting the injection barrier.

4.5 Total Current Collapse in GaN Diodes

In this section, total current collapse phenomena in GaN SBDs and GET-SBDs are studied. During the pulse stress, the substrate was in floating condition to avoid the impact of early buffer (UID buffer) breakdown on the results. The influence of substrate polarity connection on the dynamic characteristics of AlGaN/GaN diode will be addressed in section 5.3.5 of chapter 5. The current transient methodology is used in this section to extract the trap information which is defined in a 2-dimensional TCAD simulator to understand the voltage-dependent trapping characteristics. Finally, a solution to suppress the total current collapse is proposed and presented.

4.5.1 Total Current Collapse and Physical Origin

With the reverse voltage increases, the depletion region in the GaN diodes extends in the lateral direction. According to the Poisson's equation (4.4) below,

$$-\nabla^2\psi = \nabla\cdot\mathbf{E} = \frac{\rho}{\varepsilon} \tag{4.4}$$

the peak electric field at the junction edge increases. This can lead to further band bending at the anode edge and electron filling of shallower trap states. In Figure 4.10(a) and (b), typical pulsed *I*–*V* characteristics of SBD and GET-SBD with stressing pulse down to −200 V are shown. In the case of conventional SBD, the forward current is totally collapsed when the diode is subject to a stress pulse higher than 175 V. This phenomenon is regarded as "total current collapse" (TCC). In Figure 4.10(a), two regimes have been observed in terms of current levels: gradual current reduction before a critical voltage and total current collapse when V_R goes beyond the critical voltage. Before reaching the critical voltage of $V_R = -175$ V in this measurement, the diode can still turn on around 1.5 V (with criteria of I_F = 1 mA/mm after normalization of the current to the width of the Anode finger). It is clearly observed that there is a gradual reduction of maximal forward current at V_F of 2.5 V by increasing the reverse bias from 0 V to −150 V, which is correlated with the increase of on-resistance as calculated in Figure 4.10(c). Moreover, the totally collapsed current can still abruptly jump to the "normal" level when a sufficiently high forward voltage is applied. The hypothesis for this phenomenon is that the forward voltage applied at the anode contact triggers the de-trapping of states in the vicinity of the contact, and the total current collapse is associated with the Fermi-level pinning at the trap level [3].

In Figure 4.10(b), the pulsed characteristics of the GET-SBD are very similar with the ones of the SBD in Figure 4.10(a). The comparison of dynamic R_{ON} increase with stressing voltage for the SBD and the GET-SBD is summarized in Figure 4.10(c). As is displayed, the GET-SBD shows lower dynamic R_{ON} increase compared with conventional SBD. This can be explained by a lower electric field at the anode edge, as is shown in Figure 4.10(d). In Figure 4.10(d), the X coordinate at 0 corresponds to location at the Schottky contact edge. However, the total current collapse phenomena can be observed in the GET-SBD as well. The Fermi-level de-pins due to the positive voltage applied, and the diode shows an abrupt turn-on characteristic.

As is seen in Figure 4.10(a) and (b), the characteristics for the SBD and the GET-SBD are very similar, though the electric field distribution is different. The pinning and de-pinning characteristics indicate that there exists trapping/de-trapping effects in the vicinity of the Schottky contact. Since the de-pinning effects were triggered by the positive potential at the anode contact with small voltages, it points out that the trapping zone is very close to the contact. Otherwise, the de-pinning phenomenon cannot take place.

[3] The Fermi-level pinning corresponds to the situation when severe electron trapping occurs at the defect level. The conduction band is lifted up due to the electrostatic effect, and the 2DEG is completely depleted even after the removal of the stress voltage. This causes a total current collapse of the GaN diode.

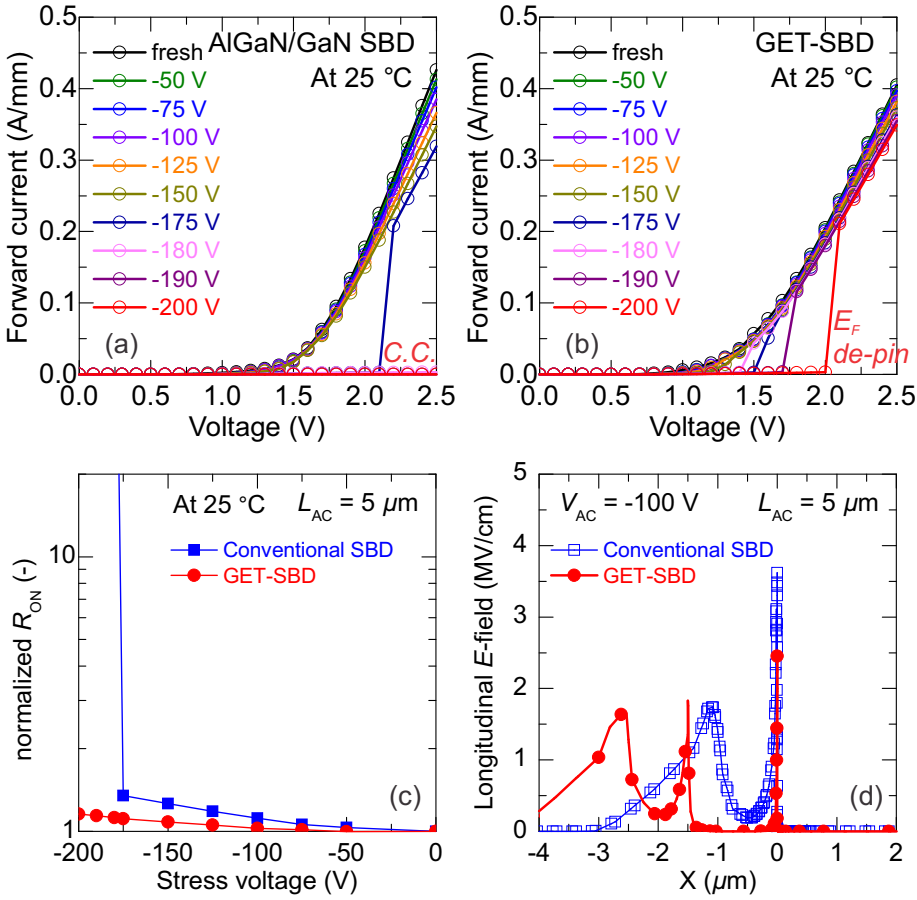


Figure 4.10: Pulsed *I*–*V* characteristics of SBD (a) and GET-SBD (b) with filling pulse down to −200 V, a total current collapse phenomenon occurs when the diodes are subject to a stress voltage of −200 V. The sudden current increase in both diodes corresponds to the Fermi-level de-pinning phenomenon triggered by the positive pulse applied at the anode. (c) The normalized R_{ON} of SBD and GET-SBD with stressing pulse voltages (if the diode can suddenly turn on, the R_{ON} was calculated in the linear region as well). (d) The simulated longitudinal electric field in conventional AlGaN/GaN SBD and GET-SBD at V_R of −100 V.

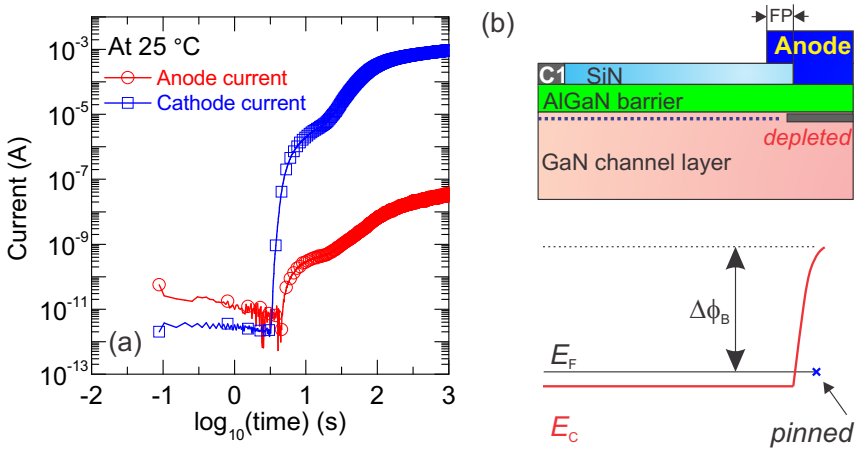


Figure 4.11: (a) The Cathode and Anode currents during the current transient measurements performed at 25 °C. (b) The schematic of the stressed AlGaN/GaN SBD and the conduction band profile of the 2DEG under the Fermi-level pinning condition.

To verify the pinning and trapping effects, a current transient measurement has been performed on the conventional SBD by using the methodology introduced in section 4.4.1. The results are shown in Figure 4.11. The Cathode and Anode currents were both plotted in Figure 4.11(a). The Cathode current is several orders of magnitude higher than the Anode leakage current after 10 s. The trap spectra have been extracted from the data of the Cathode current. It is noticed that the Cathode current increases 5 orders of magnitude in a time window of 3–10 s. This is indicative of the Fermi-level de-pinning causing a significant increase of the 2DEG density and current. The Anode current (i.e. the leakage current) also increases at that time, since the injection barrier reduces. From the characteristics of the Cathode current transient, it can be concluded that there is more than one trap involved during the trapping/de-trapping stages.

The Fermi-level pinning/de-pinning effects can be understood in Figure 4.11(b). There is a strong trapping occurring at the corner of the Schottky contact during stressing, the Fermi-level is pinned at this trap level pulling up the conduction band of the GaN channel. After removal of the stress voltages, the 2DEG at the access region will be replenished from the Cathode contacts. Due to the strong virtual gate effect, the 2DEG under the Schottky metal stays depleted. This is due to the additional barrier created in the GaN channel by the Fermi-level pinning. In Figure 4.11(b), the bottom right graph shows the schematic conduction band profile in the 2DEG GaN channel of the stressed SBD. Due to the Fermi-level pinning at the corner of the Schottky contact, an additional energy barrier $\Delta\phi_B$ is created, impeding the replenishment of the 2DEG into the location underneath the anode metal. In the access region, the 2DEG is replenished

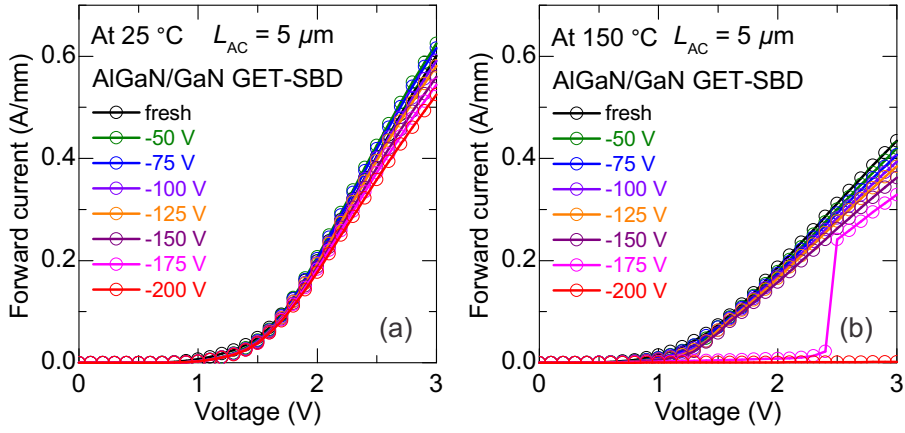


Figure 4.12: Pulsed *I–V* characteristics of GET-SBD with substrate connected to anode measured at 25 °C (a) and 150 °C (b).

and present. The Fermi-level E_F is moving into the conduction band again. Basically, it is the additional barrier $\Delta\phi_B$ causing the total current collapse in the diodes. For a fresh AlGaN/GaN SBD, the turn-on voltage is determined by the barrier height. This additional barrier causes the diode to turn-on at much higher voltage. However, when a sufficiently high forward voltage is applied at the anode, it can assist the de-trapping of the filled states. When the electrons are released from the trapped states, the Fermi-level moves into the conduction band again. The additional barrier $\Delta\phi_B$ disappears, resulting in a sudden turn-on characteristic or a feature of "jump" in current in both SBD and GET-SBD. The total current collapse can also be understood by a highly resistive zone created below the Schottky contact, causing a tremendous increase of the R_{ON}. In this view, 2DEG variation and R_{ON} increase align with the model of virtual gate effects due to the trapping effects.

4.5.2 Impact of Substrate Connection

Due to the low BV (below 200 V) of UID-buffer in the negative polarity, the pulsed *I–V* measurements on the diodes were performed with substrate floating. However, the buffer BV in the positive polarity can go beyond 200 V [90]. In this case, the Si substrate can be connected to the anode contact while switching the cathode contact in pulsed mode. More detailed discussion of the substrate connection can be found in section 5.3.5 of chapter 5. In this section, we explore the pulsed *I–V* characteristics of GET-SBD (with substrate connected to the anode contact) at 25 °C and 150°C.

Figure 4.12(a) and (b) show the typical *I–V* characteristics of GET-SBD at 25 °C and 150 °C. At 25 °C, the AlGaN/GaN GET-SBD after a pre-bias at −200 V shows no total current collapse any more when the substrate is shorted with the anode contact. The reason is that the lateral electric field is lower when the substrate potential is forced

to the ground than the situation where the substrate is in floating condition. However, the measurements at 150 °C still show the total current collapse and the curve with Fermi-level de-pinning. It is possible that more severe electron trapping occurs at high temperature than at room temperature. In order to solve this total current collapse issue in both SBD and GET-SBD, it is essential to remove this "detrimental trap". The improved results will be shown at the end of this chapter.

4.5.3 Trapping Analysis and TCAD Simulations

In order to verify the strong pinning at the corner of the Schottky contact, trap occupancy has been simulated in a two-dimensional TCAD deck. Figure 4.13 shows how the two trap levels were extracted based on the current transient measurements. In the TCAD simulator, two traps (donor-like) have been defined at the Si_3N_4/AlGaN interface with a uniform spatial distribution in density. The traps were defined as bulk traps located in a small region close to AlGaN surface (0.5 nm) which allows for a clearer visualization of the trap occupation under different bias conditions. There are no trap states defined at the Anode metal/AlGaN barrier interface. The densities of the donor traps are set as 1.25×10^{12} cm^{-2} and 2.1×10^{13} cm^{-2} at "Trap1" and "Trap2" with their energy levels extracted from the current transient measurements at different temperatures as shown in Figure 4.13.

Figure 4.14(a) shows the simulated band diagram and the 2DEG density (to the right axis) at equilibrium state. The two trap levels, located at the Si_3N_4/AlGaN interface, are sitting above the Fermi-level and are thus unoccupied. Donor traps carry a positive charge when ionized and stay neutral when occupied with an electron. This means that the two trap states are ionized and positively charged, in TCAD the trap occupancy in this case is equal to "1". The normalized ionization of the two traps in our TCAD deck is shown in Figure 4.14 (b) to be "1", i.e. all the interface traps are ionized with positive charges which compensates the negative polarization charges at the AlGaN surface and gives rise to a high 2DEG density in the channel shown to the right axis in Figure 4.14(a).

At low voltage range of V_R, the electrons are firstly captured by "TP1" due to their lower energy as shown in Figure 4.15(a). With the increase of negative bias, there is a rise of the peak lateral electric field which results in more electron trapping in the vicinity of the Schottky contact. The simulated band diagram (at a distance of 0.5 nm from the Anode metal) at $V_R = -150$ V is shown in Figure 4.15(b). It is illustrated in the figure that the quasi-Fermi level is pinned at the Trap1 energy level with electrons occupying those deeper trap states. The Trap2 is still located above the quasi-Fermi level and remains ionized. Due to the relatively low density of Trap1, the 2DEG channel can still be formed when a pulsed forward voltage is applied.

TCAD simulation results obtained using the trap occupation described in Figure 4.15(c) have supported the hypothesis that the trapping phenomena occurred at the corner of the Schottky contact, and a lateral extension of trapped region for "Trap1" was observed when the reverse bias becomes more negative. The occupied donor states induces a field effect which reduces the density of 2DEG resulting in a higher on-resistance as observed from experimental data shown in Figure 4.10(c). The "Trap2" stays ionized

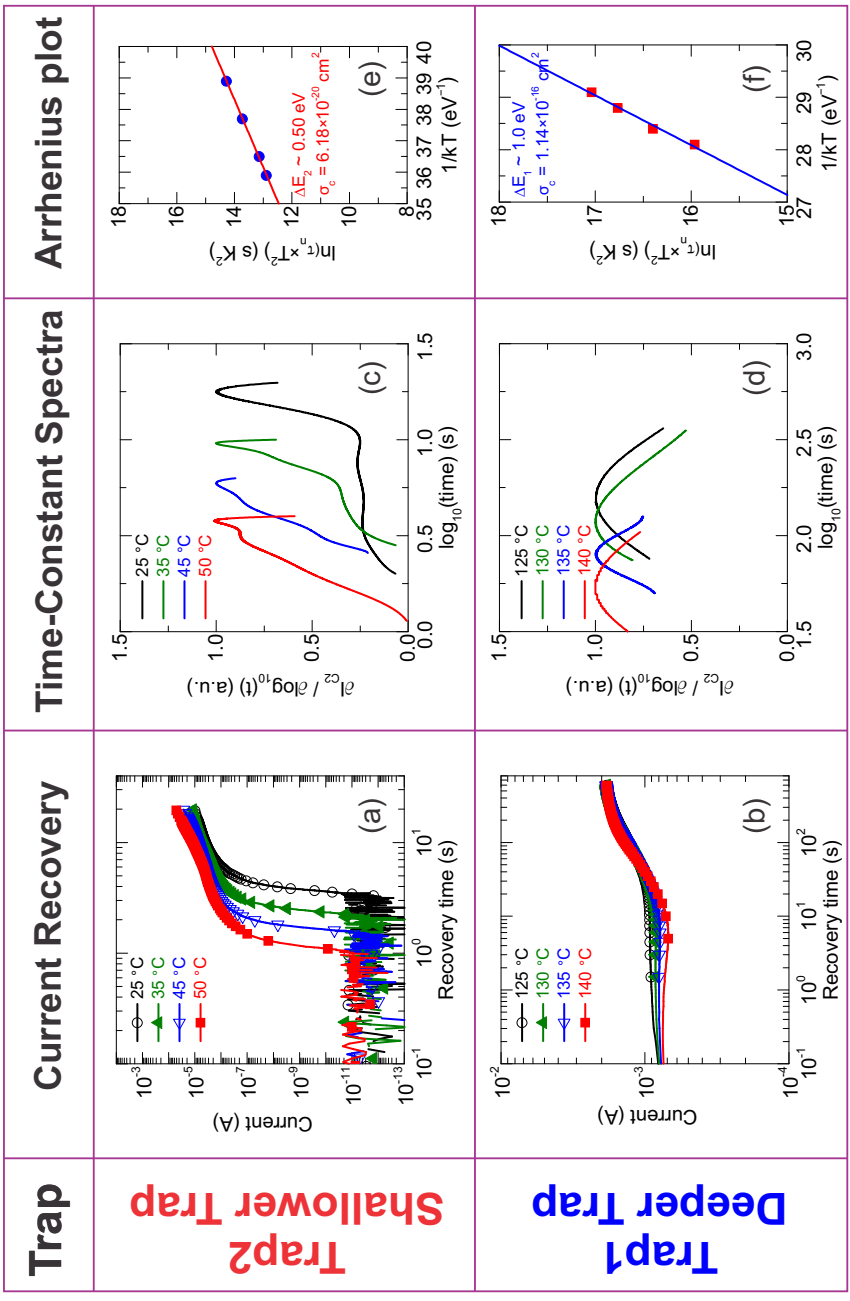


Figure 4.13: The extraction of the trap information for TP1 and TP2.

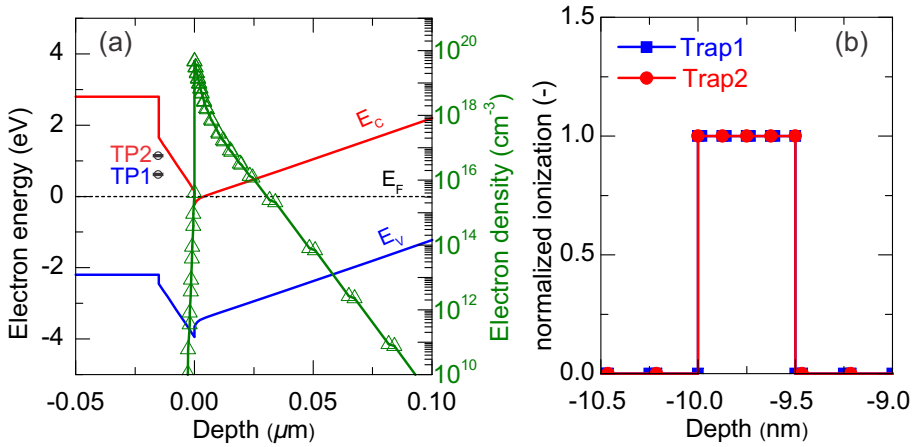


Figure 4.14: (a) The simulated band diagram and 2DEG density at equilibrium, TP1 and TP2 are defined at the Si_3N_4/AlGaN interface. (b) Normalized ionization of the two traps by taking a vertical cut-line at the access region.

till $V_R = -150$ V.

At even more negative bias, "Trap2" starts to be filled with injected electrons due to the further bending of the band laterally. The simulated band diagram (at $V_R = -175$ V) in Figure 4.16(a) shows that the quasi-Fermi level at the Si_3N_4/AlGaN interface is pinned at the trap level of 0.5 eV, which demonstrates the charging effect at the energy level of "Trap2". The normalized ionization from simulation in Figure 4.16(b) confirms the process of electron-filling at "Trap2" at more negative bias (the simulated $V_R = -175$ V), since the normalized ionization of "Trap2" starts to drop. With the increase of the stress voltage, the normalized ionization of "Trap2" keeps dropping. When it is fully filled, the current can be blocked at the forward regime before the discharging of these trapped states and de-pinning of the Fermi-level take place.

From the measurement results shown in Figure 4.10, there is a jump of current when the device was stressed with V_R of -175 V. This is a signature of de-pinning of the Fermi-level at the Si_3N_4/AlGaN interface with a distance of several nanometers from the corner of Schottky contact where a positive pulse voltage was applied. Most importantly, this phenomenon of Fermi-level de-pinning can only take place at a limited distance from the Anode metal, since the jump of current is triggered by a "small" positive voltage.

4.5.4 Suppression of Total Current Collapse

From the discussion in previous subsection, the total current collapse phenomena in GaN SBD and GET-SBD result from electron trapping at the anode corner. It

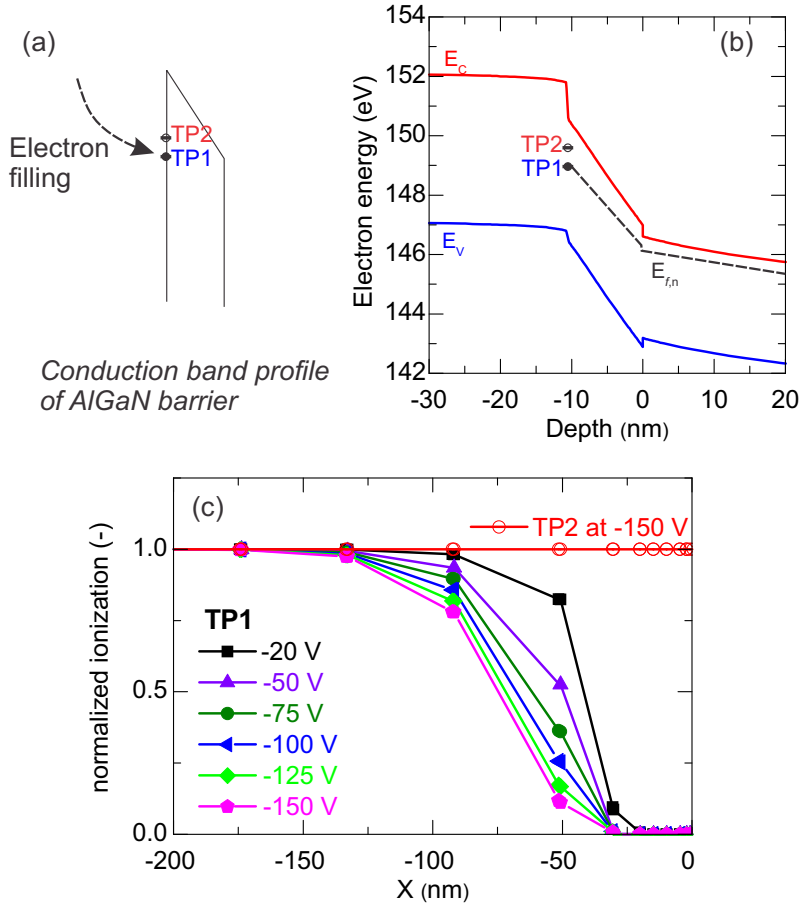


Figure 4.15: (a) The schematic of conduction band profile of AlGaN barrier with electron filling of Trap1. (b) Simulated band diagram at voltage V_R = −150 V. The lateral distribution of normalized ionization for "Trap1" with different V_R down to −150 V and for "Trap2" at V_R = −150 V. The position of X = 0 nm corresponds to the corner of the Schottky contact.

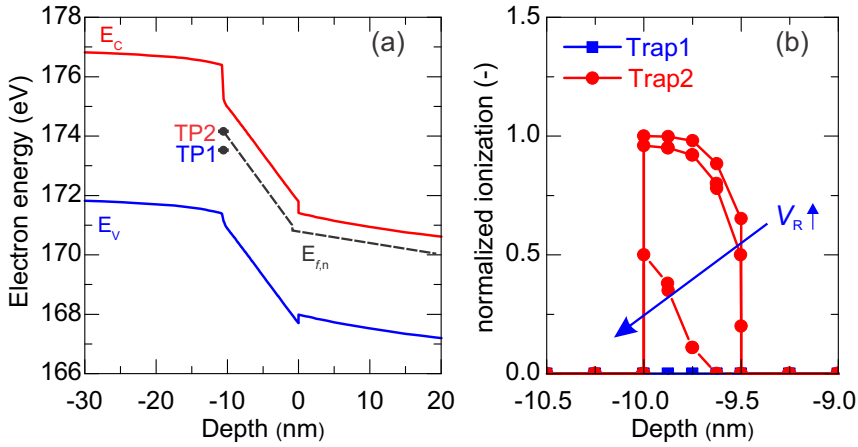


Figure 4.16: (a) The simulated band diagram at$V_R = -175$ V. (b) Normalized ionization of the two traps defined at the Si_3N_4/AlGaN interface, it also illustrates the further electron filling of Trap2 with increase of V_R.

is possible that the total current collapse of both architectures originates from the same source: trap at the AlGaN/RTCVD-Si_3N_4 interface. To solve this issue, we used different Si_3N_4 in the access region and in the gated edge termination structure. Figure 4.17(a) and (b) show the new cross-section of AlGaN/GaN SBD and GET-SBD, respectively. In the access region, *in-situ* Si_3N_4 is used for passivation the AlGaN surface. In the GET-SBD, the *in-situ* Si_3N_4 is removed in the anode trench before the deposition of gate dielectric. In the new GET-SBD structure, PEALD-Si_3N_4 is used as the gated edge termination instead of RTCVD-Si_3N_4. In the region between the GET and the cathode contact, *in-situ* Si_3N_4 remains as the passivation layer in the GET-SBD architecture.

Figure 4.17(c) and (d) show the cross-sectional TEM images for AlGaN/GaN heterostructure with RTCVD and *in-situ* Si_3N_4 as the passivation layers. For Si_3N_4 far away from the Si_3N_4/AlGaN interface, the material reveals to be in amorphous state, regardless of the deposition techniques. However, the *in-situ* Si_3N_4 near the AlGaN surface shows crystalline fringes in the TEM image in Figure 4.17(b). Lu *et al.* [91] presented that remarkable reduction of the trap states at SiN/AlGaN interface have been achieved by using *in-situ* Si_3N_4 as the gate dielectric for GaN MISHEMTs. From the X-ray photoelectron spectroscopy (XPS) analysis on the *in-situ* Si_3N_4, the N/Si ratio (1.29) exhibits closer to the ideal value of 1.33 compared with previously reported results (1.21 and 1.25) [92, 93]. Figure 4.17(e) presents the D_{it} at the Si_3N_4/AlGaN interface for two Si_3N_4: the RTCVD-Si_3N_4 and the PEALD-Si_3N_4 [94]. The extracted D_{it} is significantly lower for device with PEALD-Si_3N_4 ($D_{it} \sim 1\times 10^{11}$–$2.3 \times 10^{12}$ $cm^{-2}eV^{-1}$) than for the one with an RTCVD-Si_3N_4 ($D_{it} \sim 3.3\times 10^{13}$–$3.5 \times 10^{13}$

$cm^{-2}eV^{-1}$) as the gate dielectric [94]. In the new SBD and GET-SBD architectures, better Si_3N_4/AlGaN interface is achieved. It is expected that the the total current collapse phenomenon can be mitigated.

In Figure 4.18(a) and (b), the pulsed forward *I–V* characteristics with pre-bias of −200 V for the AlGaN/GaN SBD and GET-SBD with different Si_3N_4 at the corner of the Schottky contact are shown. Due to a strong trapping for diodes with RTCVD passivated AlGaN surface, the forward current can be totally collapsed in the case of both SBD and GET-SBD. With *in-situ* Si_3N_4 as the passivation layer, lower interfacial trap states can be achieved. The results show that the total current collapse and Fermi-level pinning effect have been suppressed by using *in-situ* Si_3N_4 in AlGaN/GaN SBD (Figure 4.18(a)). In the case of AlGaN/GaN GET-SBD, the Si_3N_4/AlGaN interface was improved by selecting PEALD-Si_3N_4 as the material for gated edge termination. Figure 4.18(b) shows that the total current collapse phenomenon and Fermi-level de-pinning curve are suppressed in the new AlGaN/GaN GET-SBD. The improvements in both AlGaN/GaN SBD and GET-SBD validate that the collapsed currents are due to the severe trapping mechanism at the anode edge (at the interface of RTCVD-Si_3N_4 and AlGaN barrier). However, it should be noted that the forward currents of SBD and GET-SBD after a stress pulse at −200 V are still much degraded, compared with the fresh condition. This degradation is related to dominant buffer trapping instead of a surface-related issue. Dedicated discussion of buffer trapping impacting the GaN diode stability will be performed in chapter 5.

4.6 Summary and Conclusions

In typical DC/DC power converters, GaN diodes switch passively between OFF and ON states when the transistor is actively changing its states. During the OFF-state operation, the high electric field condition can induce electron injection and trapping at various locations, impacting the dynamic characteristics of GaN diodes. In the second section of this chapter, a new pulsed *I–V* measurement procedure was proposed to mimic and characterize the dynamic characteristics of GaN diodes in switching circuits.

It leads to further trapping analysis of the GaN diodes showing bias-dependent dynamic R_{ON} increase under pulsed *I–V* measurements for both conventional AlGaN/GaN SBDs and GET-SBDs. Besides a gradual current reduction, the GaN diodes showed total current collapse phenomena and sudden turn-on characteristics. A model of surface electron trapping and Fermi-level pinning was proposed to interpret the data, that has been verified by the current transient measurements.

Finally, an *in-situ* Si_3N_4 grown in a MOCVD chamber has been used as the passivation layer. Due to its growth environment, *in-situ* Si_3N_4 layer typically is denser than RTCVD Si_3N_4 and contains lower hydrogen. The *in-situ* Si_3N_4 was reported to have a close to ideal Si/N ratio. All this information indicates that the *in-situ* Si_3N_4 can lead to better interfacial quality of the Si_3N_4/AlGaN interface. In the case of GET-SBD, PEALD-Si_3N_4 as the new material was used in the gated edge termination. In the remaining access region, the AlGaN surface was passivated with *in-situ* Si_3N_4 as well.

From the pulsed *I–V* measurements, the total current collapse phenomena and Fermi-

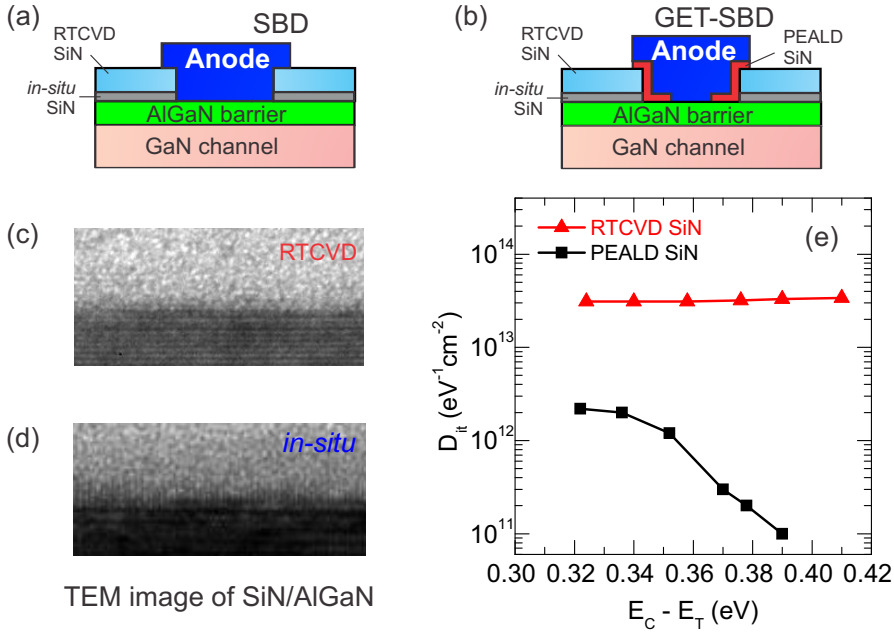


Figure 4.17: (a) The cross-section of conventional AlGaN/GaN SBD with an *in-situ* Si_3N_4 as the passivation layer in the access region. (b) The cross-section of conventional AlGaN/GaN GET-SBD by using an *in-situ* Si_3N_4 as the passivation layer in the access region and a PEALD Si_3N_4 as the gated edge termination. (c) The transmission electron microscopy (TEM) images of AlGaN/GaN heterostructure with RTCVD-Si_3N_4 passivated AlGaN surface. (d) The TEM image of AlGaN/GaN heterostructure with *in-situ* Si_3N_4 passivated AlGaN surface (*courtesy: Dr. M. Zhao, imec*). (e) D_{it} values at the Si_3N_4/AlGaN interface extracted from the frequency dependent conductance technique for RTCVD Si_3N_4 and PEALD Si_3N_4, respectively (*replotted from [94]*.

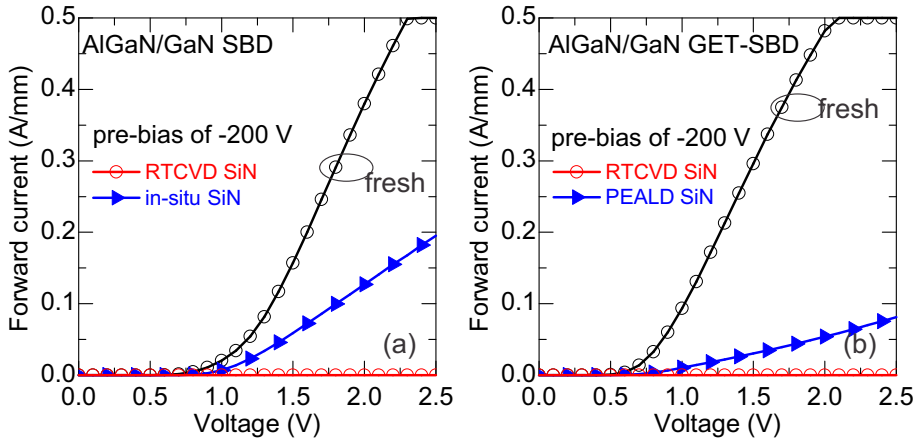


Figure 4.18: (a) The suppression of current collapse in AlGaN/GaN SBD by using *in-situ* Si_3N_4 as the passivation layer. (b) The suppression of current collapse in AlGaN/GaN GET-SBD by using PEALD-Si_3N_4 in the GET structure and the *in-situ* Si_3N_4 as the passivation layer in the access region.

level pinning effects have been suppressed for both AlGaN/GaN SBD and GET-SBD with new Si_3N_4 dielectrics. It further gives validation for the TCAD model based on the current transient measurements.

Chapter 5

Effects of Buffer Trapping on GaN Diodes

In this chapter, extensive trapping analysis has been performed on GaN diodes, fabricated on intentionally carbon-doped buffer layers. The carbon-doped (Al)GaN buffer can effectively suppress the buffer parasitic leakage current, however, it can potentially degrade the stability properties of the GaN diodes. To identify the buffer trapping mechanism, current transient measurements on SBD and TLM structures were performed. TCAD simulation was used to analyze the trapping effects in AlGaN/GaN diodes with edge termination. Finally, a significant improvement of the stability of GaN diodes is achieved by using a low-trapping buffer for the fabrication of GaN diodes.

5.1 Introduction

To enable low-cost fabrication of GaN-based electronic devices, the growth of AlGaN/GaN epi-layers on large-area silicon substrates has been developed [13,15,95]. The GaN-on-Si growth is typically achieved by metal organic chemical vapor deposition (MOCVD). Due to the large lattice and thermal expansion coefficient mismatch between (Al)GaN and silicon, the growth of high-quality crack-free AlGaN/GaN epitaxial layers on 200-mm silicon substrates requires intensive optimization of the growth parameters and design of the layers in terms of layer thickness, Al% in the buffer layers, etc [96].

In many cases, the breakdown voltage of GaN-based HEMTs and SBDs can be limited by the buffer leakage current when it exceeds a commonly used value of 1 mA/mm [60]. This phenomenon was discussed as well in section 3.2.1 of chapter 3. The parasitic buffer leakage is strongly related to the crystal defects (unintentional dopants, point defects, etc.) generated during the growth in a MOCVD reactor. It was reported that the unintentional doped (UID) GaN showed n-type conductivity, and the carrier density can exceed 10^{16} cm^{-3} [97]. Van de Walle *et al.* proposed that the n-type donors in UID GaN originate from the unintentional impurities such as oxygen and silicon, based on first-principles calculations [57]. The activation energy of Si in GaN is $\sim$ 30 meV [98]. It is important to note that the incorporation of those n-type donors as the background dopants into the GaN lattice is difficult to avoid, for instance, silicon can come from the quartz parts of the growth reactors [99].

To suppress the buffer leakage, a stack of high-quality insulating buffer layers is essential to block the vertical leakage path. The utilization of a carbon-rich (Al)GaN

buffer for the device fabrication proves to be an effective approach of obtaining a highly resistive buffer. Many research groups have optimized the growth conditions to intentionally incorporate carbon into the GaN buffer layers [60, 100]. Carbon acts as an acceptor-like agent compensating the unintentional n-type dopants. Thus, the Fermi-level in the buffer is moved to the mid-gap obtaining a semi-insulating buffer.

The incorporation of carbon into the (Al)GaN buffer can be controlled by the growth pressure [101, 102] or the growth temperature [58], etc. But during the epitaxial growth with a carbon-doped buffer, traps can be created impacting the dynamic stability of the devices. An extensive trapping study has been performed on GaN HEMT with intentional carbon doped buffer, to study the trade-off between dynamic R_{ON} and off-state leakage [103].

In this chapter, an extensive trapping analysis on AlGaN/GaN SBDs and GET-SBDs fabricated on carbon doped buffers is presented. Current transient measurements are performed on the SBDs and transmission line (TLM) structures based on AlGaN/GaN heterostructures, to have a spatial identification of the traps. TCAD simulations are performed to understand the buffer trapping mechanism in the GET-SBD architecture. Finally, a significant improvement of dynamic characteristics of the GET-SBD is shown by properly designing a low-trapping buffer for the device fabrication.

5.2 Intentional Carbon Doped Buffer

This section will briefly show the motivation of intentional carbon-doped buffers and the comparison of electrical results for GET-SBD with UID and carbon-doped buffer.

5.2.1 Motivation of Intentional Buffer Doping

During the epitaxial growth of an AlGaN/GaN heterostructure in a MOCVD chamber, there are contaminations of O, Si, H, C, etc. in the system, making the buffer layers unintentionally n-type doped. The n-type buffer can potentially increase the overall leakage current due to a dominant buffer leakage to the conductive substrate and degrade the breakdown voltage [104].

To increase the buffer resistivity, intentional buffer doping with Fe or C was utilized. The intentional dopants such carbon introduce acceptor-like trap states, so that the Fermi-level is pinned closer to the valence band and the material is slightly p-type [59]. However, iron doping in the (Al)GaN suffers from a memory and segregation effect, making it difficult to precisely control the doping profile [61, 105]. Moreover, to minimize the trap levels close the the 2DEG channel, it is better to use the carbon doping compared with iron-doping to obtain a semi-insulating buffer [59].

To control the carbon concentration profile in the (Al)GaN layer, Chen *et al.* demonstrated a temperature-tuned technique to optimize the carbon profile in the GaN buffer layer [61]. As shown in Figure 5.1(a), a stack of GaN layers on an AlN nucleation layer was designed and grown at different temperatures. Secondary Ion Mass Spectrometry (SIMS) was performed to evaluate the dopant concentration. In Figure 5.1(b), it explicitly shows that the carbon profile follows exactly the temperature variations. By

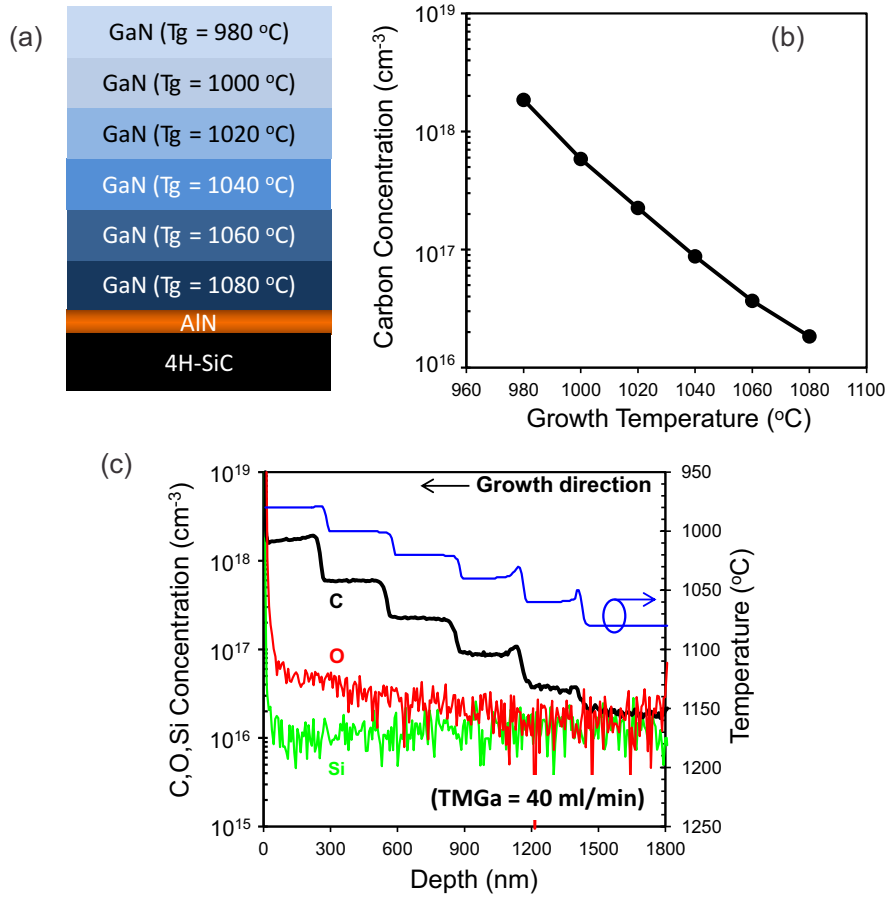


Figure 5.1: (a) Schematic cross section of the growth structure with GaN layers grown at various temperatures. (b) The carbon concentration versus growth temperature. (c) The dopants (Si, O, C) SIMS profile versus growth temperature. *Reprinted from* [61].

lowering the growth temperature, the carbon incorporation into the lattice increases remarkably. A possible physical mechanism for this can be found in the work by Parish *et al.* [106]. It was proposed that carbon was removed from the reaction surface by the conversion of methyl groups from TMGa into methane by reacting with adsorbed hydrogen atoms as the temperature is raised [106]:

$$CH_3(ad) + H(ad) \rightarrow CH_4(g). \tag{5.1}$$

It should be noted that Carbon contamination always exists even when the growth temperature is as high as 1080 °C. By lowering the growth temperature from 1080 to 980 °C, the carbon concentration in the GaN layer increases from $\sim 1.8\times10^{16}$cm^{-3} to $\sim 2.0\times10^{18}$cm^{-3} [61]. In Figure 5.1(c), the SIMS profiles for C, O, and Si are shown versus the depth, which is correlated with the growth temperature. It shows that the residual O and Si concentration is less temperature dependent compared with the carbon incorporation.

By the work from *Chen*, the temperature-tuned carbon incorporation in the GaN buffer is shown to be an effective approach. This method will be used to increase the carbon concentration in AlGaN buffer layer as a back-barrier in AlGaN/GaN Schottky barrier diodes.

5.2.2 Electrial Characteristics and Discussion

To better confine the electrons in the 2DEG and reduce the leakage from source to drain (punch-through effect), an AlGaN buffer was used as a back-barrier due to an increased conduction band off-set compared with the GaN channel. Additionally, an intentionally carbon doped buffer was introduced to obtain a semi-insulating buffer. In the growth of AlGaN, ammonia was used as the nitrogen precursor instead of TMGa. However, the principle of temperature-tuned carbon incorporation is the same as discussed in previous section.

In Figure 5.2(a) and (b), the cross-sections of two epi-stacks for diode fabrication are shown. The buffer layers in both UID buffer and C-doped buffer consist of three step-graded layers. In the C-doped buffer, only the top $Al_{0.08}Ga_{0.92}N$ layer was intentionally carbon doped, which was grown at 980 °C compared to 1040 °C for the growth of the UID buffer. Based on the SIMS profile, the carbon concentration in the $Al_{0.08}Ga_{0.92}N$ layer is $\sim 2\times10^{19}$cm^{-3} compared to the value of $\sim 12\times10^{16}$cm^{-3} in the UID layers grown at higher temperatures [1]. The capping layer of the wafer was 5-nm Si_3N_4 grown in the MOCVD chamber. The entire stack was then encapsulated by 140 nm Si_3N_4 layer by means of rapid thermal chemical vapor deposition (RTCVD). The removal of the Si_3N_4 passivation layer was performed by SF_6 dry etching. The Au-free anode metal was composed of a TiN-based stack, and a stack of Ti-based metals was used for the cathode contact formation [29].

[1] Thanks to Dr. M. Zhao, imec, for the development of the growth techniques. It should be noted that the carbon incorporation can be influenced by many growth parameters: precursor, growth temperature, pressure, etc. The solubility of carbon in GaN and AlN is reported to be excellent (i.e. 10^{20}cm^{-3} or even higher) [107]

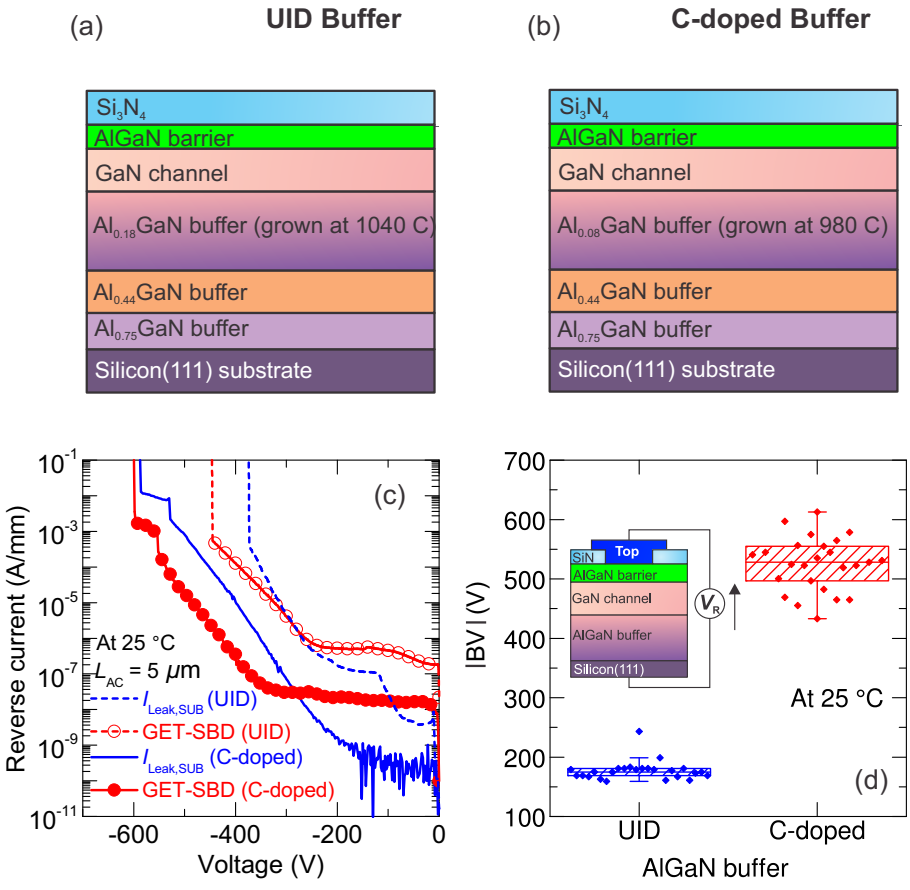


Figure 5.2: Schematic cross-section of the epitaxial layers for a UID buffer (a) and an intentionally carbon-doped AlGaN back-barrier (b) which was grown at a relatively low temperature. (c) The buffer leakage current and GET-SBD leakage current (at 25 °C) measured on a UID and C-doped buffer, respectively. (b) Statistical evaluation of the vertical buffer BV for UID and C-doped AlGaN buffers.

To investigate the impact of the carbon-doped AlGaN buffer on the leakage current of GET-SBD, the off-state electrical characterization was performed on GET-SBDs fabricated on UID and C-doped buffers, respectively. The result is shown in Figure 5.2(c), where the buffer parasitic leakage current is suppressed for the GET-SBD fabricated on C-doped AlGaN buffer layers. The vertical buffer BV was statistically assessed on dedicated structures shown in Figure 5.2(d). The top electrode in the breakdown (BD) test structure is a cathode contact (ohmic contact with the 2DEG), and the measurements were performed by applying a negative voltage at the top contact while grounding the silicon substrate. A significant improvement is found for the buffer BV in C-doped AlGaN buffer, which is also reflected in the enhancement of the diode BV as displayed in Figure 5.2(c). At low voltages (for V_R smaller than 200 V), the overall leakage current of the GET-SBD is dominated by the injection of electrons from the anode contact to the GaN channel. As the V_R further increases, the buffer leakage current shows an exponential dependence on V_R which is also reflected in the increasing leakage current of the GET-SBD. Despite the suppression of the buffer leakage and the enhancement of the buffer BV, there is still a need to further optimize the buffer for higher voltage applications due to its dominant leakage current over the diode leakage at high voltage range.

5.3 Dominant Buffer Trapping

In this section, the dynamic characteristics of the SBD and the GET-SBD fabricated on UID and C-doped buffers are compared. From dynamic pulsed *I–V* characteristics, we observed a pronounced R_{ON} degradation of the AlGaN/GaN SBDs and GET-SBDs, when they are fabricated on Carbon-doped buffers. This dynamic R_{ON} degradation causes a clear forward current reduction for the AlGaN/GaN SBDs. From combined off-state stress and current transient measurements on AlGaN/GaN SBDs, we confirm that the degraded current is recoverable and the R_{ON} degradation is due to a temporary trapping mechanism. To spatially discriminate the traps located in the buffer from the ones at the AlGaN surface, current transient measurements on AlGaN/GaN SBDs and AlGaN/GaN transmission line model (TLM) test structures were performed and compared. The results confirm that the trapping mechanism occurs in the buffer.

From the pulsed *I–V* characterization, a bias-dependent dynamic R_{ON} of the AlGaN/GaN SBD is observed. This is due to more electron filling of the same buffer trap occurring at higher stressing voltages (from −50 V to −200 V), which reflects in an enhanced current-transient amplitude at the same time-constant under higher stressing voltages. The trap level was implemented in a TCAD simulator. The simulated results in this section confirm a bulk trapping in the buffer layer for the SBD and show an additional trapped region in the GET-SBD architecture. This explains the experimental results from the pulsed *I–V* measurements.

5.3.1 Dynamic R_{ON} Instability

The dynamic characteristics of GET-SBD on two buffers have been measured by using the measurement procedure reported in 4.2.2 of chapter 4. When the AlGaN/GaN SBD

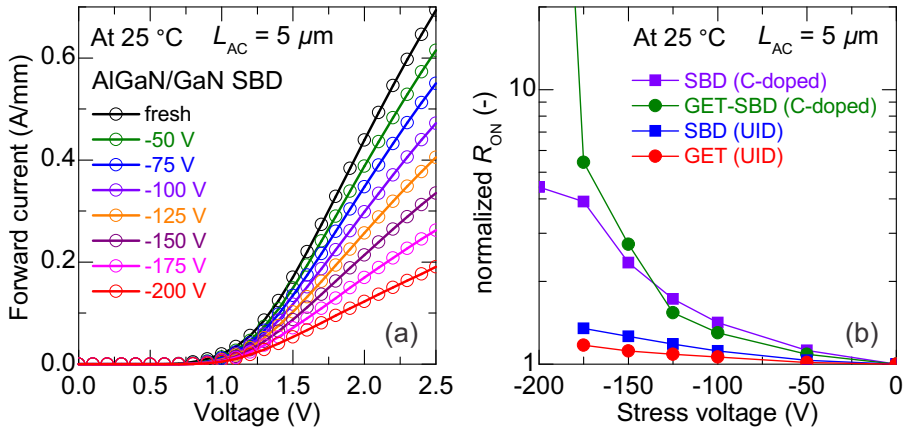


Figure 5.3: (a) Typical pulsed *I–V* characteristics of an AlGaN/GaN SBD fabricated on a C-doped buffer. (b) The normalized dynamic R_{ON} degradation for conventional SBDs and GET-SBDs on two buffers measured at 25 °C.

is subjected to a reverse voltage, the 2DEG channel is partially depleted. The electrons can be injected from the anode contact into the GaN channel and in the buffer leading to the leakage current and trapping phenomena.

Typical pulsed *I–V* characteristics of AlGaN/GaN SBDs fabricated on C-doped buffers are presented in Figure 5.3(a). With the increase of the stressing voltage V_R, there is a degradation of the forward current due to the dynamic R_{ON} increase. The bias-dependent R_{ON} increase for the reference SBD and GET-SBD on two buffers is compared in Figure 5.3(b). The GET-SBD on a UID buffer shows a slight improvement of the dynamic R_{ON} stability compared to the reference SBD on a UID buffer (4 % dynamic R_{ON} increase for GET-SBD vs 11.6 % R_{ON} increase for SBD). This can be due to the redistribution of the electric field in the vicinity of the Schottky contact [35], as has been discussed in previous chapter. The reference SBD and GET-SBD on C-doped buffers show a pronounced R_{ON} increase compared to the SBD and GET-SBD on UID buffers. This is an indication that the R_{ON} degradation is due to the C-doped buffer and C-related trap states. The GET-SBD on a C-doped buffer, with much lower leakage current than the reference SBD, did not show significant improvements in the R_{ON} stability. As seen from Figure 5.3(b), the GET-SBD suffers from a total current collapse phenomenon when the pre-bias reaches −200 V. The trapping mechanism in the GET-SBD architecture needs to be understood. From the results in Figure 5.3(b), it can already be concluded that the trapping mechanism in the GET-SBD is not related to the electric field at the anode edge. Otherwise, the dynamic R_{ON} of the GET-SBD should be more stable than that of conventional SBD.

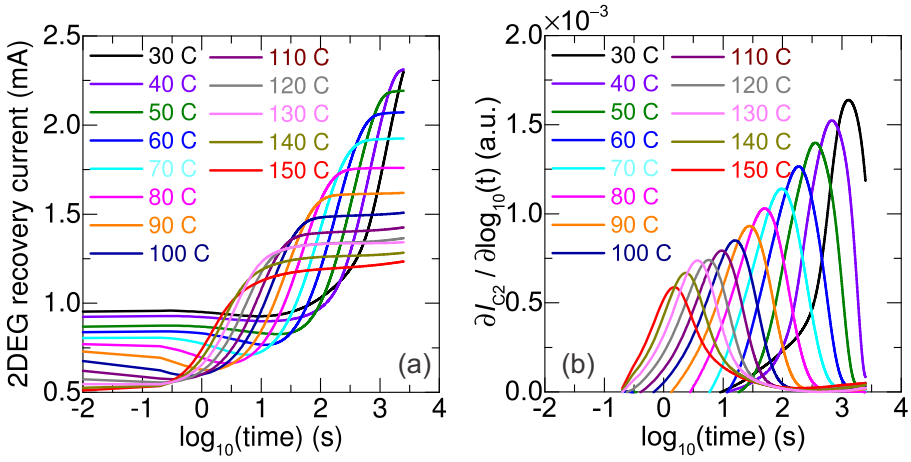


Figure 5.4: (a) The recovery current of the 2DEG channel after the diode is biased at -100 V measured at elevated temperatures. (b) The time-constant spectra at different temperatures.

5.3.2 Current Transient Measurements

To confirm and investigate the trapping mechanisms for the AlGaN/GaN SBD fabricated on C-doped buffers, we performed current transient measurements on the 2DEG resistor after a diode off-state stress at V_R of −100 V [108]. The recovery of the 2DEG current in the AlGaN/GaN SBD structure after 10-s stress at −100 V has been performed from 30 to 150 °C with results shown in Figure 5.4(a). After a recovery time of 3500 s, the SBD structure recovers back to the fresh condition (when the temperature is higher than 50 °C and the transient curves become flattened out. The time constant spectra (the derivative of the current transients) of the SBD is shown in Figure 5.4(b).

The Arrhenius plot shown in Figure 5.5 reveals the trap energy level (the slope of the fitted data) extracted from the current transient measurements performed on the SBDs fabricated on UID and C-doped buffers. There is a distinct trap level of ∼0.57 eV extrapolated on the diode with a C-doped buffer comparing with the value of 0.65 eV for SBD fabricated on a UID buffer which was previously identified as a surface trap shown in Figure 4.8 of chapter 4.

5.3.3 Spatial Identification of the Trap

In the off-state operation of the diode, electron trapping at the AlGaN barrier surface or in the GaN/AlGaN buffer layers can be induced due to the presence of both lateral and vertical electric fields in the depletion region. The trap level of ∼0.6 eV extracted in the previous section can originate from different locations. In this section, we spatially discriminate the traps located in the buffer from the ones at the AlGaN surface by performing current transient measurements on both an AlGaN/GaN SBDs and

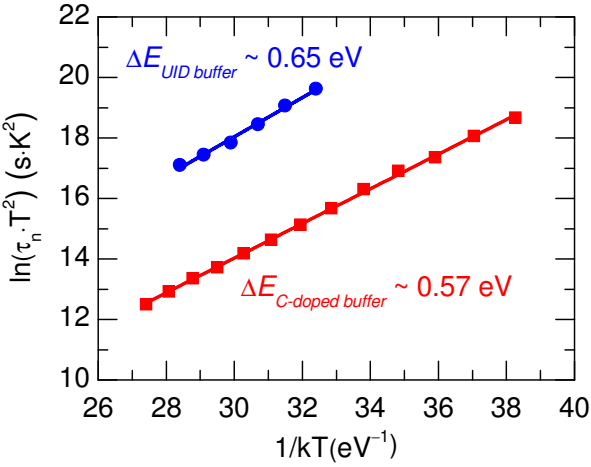


Figure 5.5: The Arrhenius plot for the diode on UID and C-doped buffers. Both diodes have been subjected to surface plasma treatment prior to the anode metal deposition.

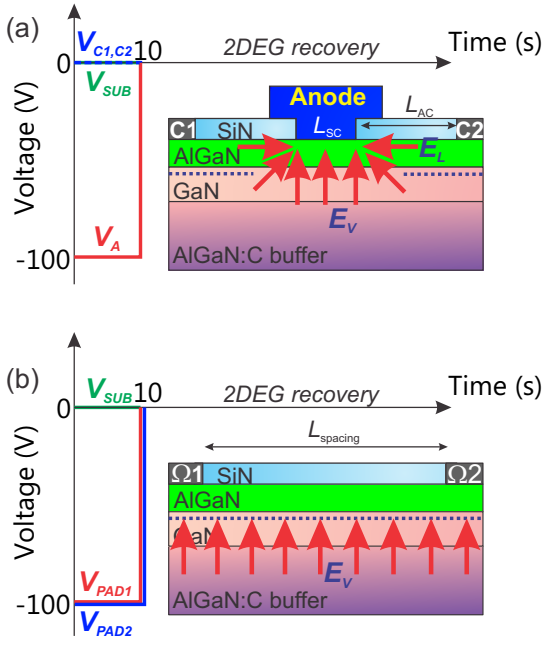


Figure 5.6: The stress procedure and corresponding electric field distribution for AlGaN/GaN SBD (a) and AlGaN/GaN TLM structure (b).

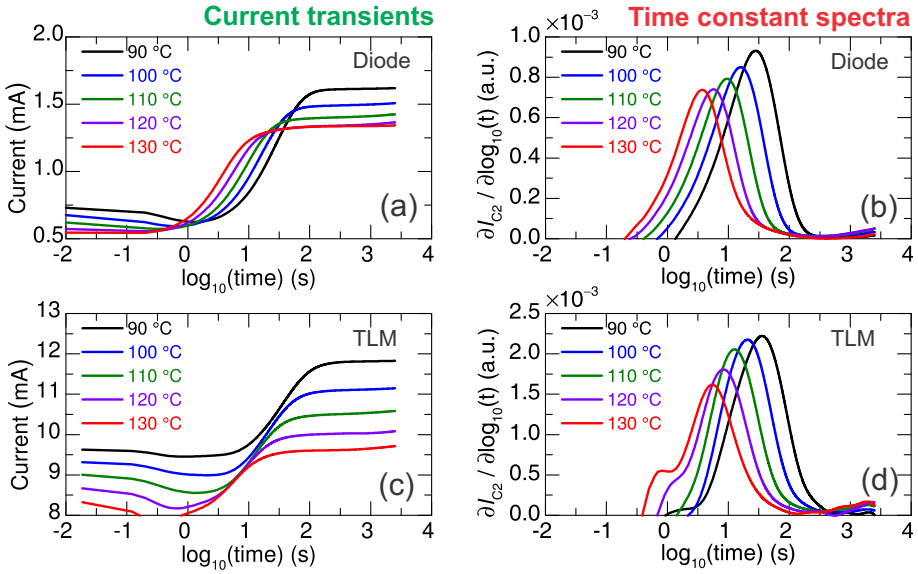


Figure 5.7: The current transient curves for a diode (a) and a TLM structure (b). The time constant spectra for a diode (c) and a TLM structure (d).

an AlGaN/GaN transmission line model (TLM) test structures. We identified buffer trapping as the dominant mechanism causing a bias-dependent trapping phenomenon in AlGaN/GaN SBDs fabricated on a buffer with intentionally C-doped AlGaN back-barrier. Furthermore, we show that the more severe R_{ON} increase of the AlGaN/GaN SBD stressed at higher voltages is due to more electron filling of the same buffer trap at the energy level of E_C−0.60 eV.

In the previous section, we used a combined technique of off-state stress and current transient measurements on the diode test structure to understand the trapping/de-trapping characteristics [108]. As is displayed in Figure 5.6(a), the anode contact is biased at −100 V with the cathode and substrate grounded during stress. In this stress state, the 2DEG channel is depleted in the vicinity of the anode contact. That creates a vertical as well as a lateral electric field which can result in electron trapping at the AlGaN surface, in the AlGaN barrier, or in the GaN channel and buffer layers. This renders it difficult to identify the spatial location of the trapping/de-trapping mechanisms. To understand the trapping mechanism shown in Figure 5.3, we used an additional AlGaN/GaN TLM test structure fabricated on the same wafer, as shown in Figure 5.6(b). The Schottky contact length (L_{SC}), the anode finger width, and the anode-to-cathode distance (L_{AC}) were 9 μm, 100 μm, and 5 μm, respectively. Thus the spacing between two cathode contacts in the AlGaN/GaN SBD is 19 μm. The AlGaN/GaN TLM test structure was composed of two ohmic contacts with a 2DEG

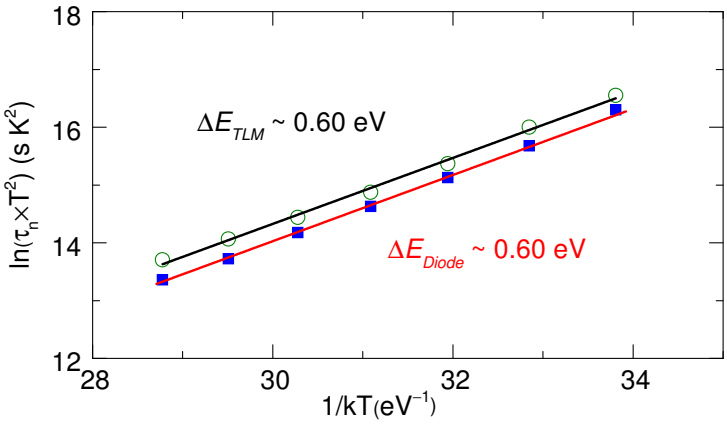


Figure 5.8: Arrhenius plot of the time constant spectra performed on the diode and TLM structure.

resistor in between and was also fabricated on the same wafer. The separation of the two ohmic pads was 6 μm. During the stress, the two Ohmic pads in the AlGaN/GaN TLM structure were biased at the same potential of −100 V. In this case, the 2DEG channel is un-depleted and in equipotential while a uniform and pure vertical E-field is generated to induce only electron trapping in the GaN channel or buffer layers (below the 2DEG).

The recovery of the 2DEG current for AlGaN/GaN SBD and TLM structure after 10-s stress have been performed from 90 to 130 °C and the results are shown in Figure 5.7(a) and Figure 5.7(b), respectively. After a recovery time of 3500 s, both the SBD and TLM structure recover back to the fresh condition and the transient curves flatten out. The time constant spectra (the derivative of the current transients) of the SBD and the TLM structure, are shown in Figure 5.7(c) and Figure 5.7(d), respectively. As is shown, the time-constant at the same temperature reveals to be almost the same for the SBD and the TLM structure. It can be noticed that the saturated current level for the Diode and the TLM at a given temperature is different, which is attributed to the different spacing between the two ohmic pads in both structures. This also results in different current transient amplitudes in Figure 5.7(c) and (d).

The Arrhenius plot for the SBD and the TLM can be generated based on the time-constants revealed in Figure 5.7(c) and Figure 5.7(d). As confirmed by the result shown in Figure 5.8, the same trap level ∼0.60 eV was extracted from the SBD and the TLM structure, respectively. This indicates that the trap causing the diode R_{ON} increase at V_{R} of −100 V is located in the buffer layers.

A cross-section 10^{-19}–10^{-21} cm^2 was obtained and reproducible on several devices. The small apparent cross-section can be explained by Hermann and Warfield's model [88, 89] in equation 4.3. It is most likely that the de-trapping mechanism of the buffer

trap states involves an additional tunneling process assisted by the defects in the buffer layers [75].

During the de-trapping process, the trapped electrons need to transport from the trapped region to the 2DEG channel. The vertical leakage path, which the carriers flow during the de-trapping process can be significantly influenced by the high-density of screw and mixed dislocations [75]. The vertical de-trapping leakage can be linked to a trap-assisted tunneling (TAT) mechanism via the defect levels in the band gap, this was reported by Uren *et al.* [75]. It is possible that this trap assisted tunneling process has an impact on the extracted cross-section. The tunneling attenuation constant λ can vary from 0.1 nm to several nm, depending on the physical location of the traps. This has a significant impact on the extracted cross-section. In literature, the reported cross-section varies from 10^{-20}–10^{-15} cm^2 [109, 110], though they all originate from the buffer-related traps.

In literature, different trap levels were extracted in AlGaN/GaN heterostructures with carbon-doped buffers [58, 84, 101]. The incorporation of carbon into the buffer was controlled by the growth pressure in Ref. [101, 102] or the growth temperature in our case and in Ref. [58], the different growth conditions can result in different trap states. The origin of this trap may not be directly related to carbon dopants but to native defects (i.e. vacancies, anti-sites, dislocations, etc.) which were generated during the epitaxial growth of the carbon doped buffer [58]. By lowering the growth temperature, we observed that the crystal quality is getting worse supported by the XRD data [111]. Tanaka *et al.* reported the trap at 0.61 eV which is a sign for nitrogen anti-site defect [102]. Though many groups have extracted a trap level ∼0.60 eV causing the recoverable degradation in GaN HEMTs with carbon doped buffer, the insight on the physical origin of this trap is still lacking. Moreover, the de-trapping kinetics may be associated with the buffer transport mechanisms which can have an impact on the extracted trap levels [75].

As shown in Figure 5.3(b), the dynamic R_{ON} of the AlGaN/GaN SBD is bias-dependent. This can be due to the electron filling of the same buffer trap or of other traps at different locations. We performed current transient measurements on AlGaN/GaN SBD structures after a reverse stress voltage (from −50 to −200 V) at 4 different temperatures (from 25 to 150 °C). The time constant spectra for the SBD stressed at 4 different voltages are presented in Figure 5.9. The curves show an enhanced current-transient amplitude at the same time constant under higher stressing voltages. This holds true for 4 different temperatures. It indicates that more trap states (at the same trap level) are filled at higher stressing voltages; that qualitatively explains the bias-dependent R_{ON} degradation in AlGaN/GaN SBDs. The inset graph in Figure 5.9 shows the same trap level of ∼0.60 eV extracted for these 4 different stressing conditions. This result suggests that the more severe R_{ON} degradation at higher stressing voltages is due to higher electron filling of the buffer trap at an activation energy of ∼0.60 eV.

To summarize, a comparison of trap spectra for AlGaN/GaN SBD and AlGaN/GaN TLM structures has been performed using combined stress and current transient measurements. We identified a single dominant E_C−0.60 eV trap in both AlGaN/GaN

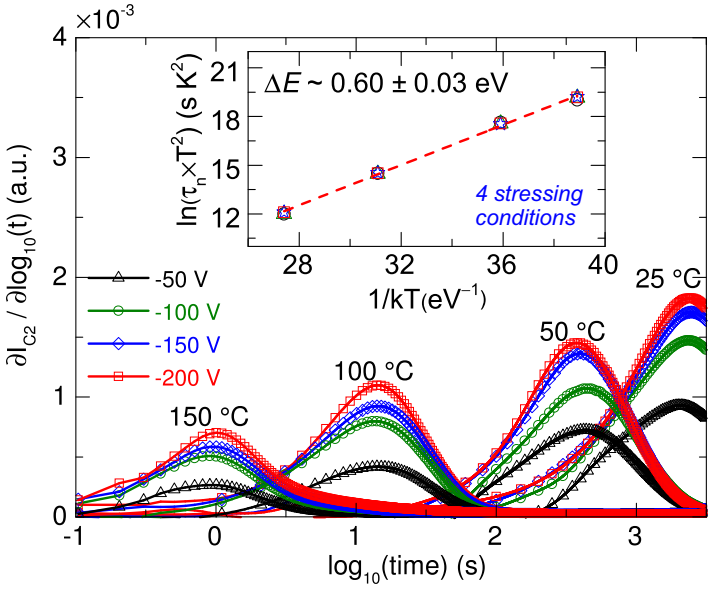


Figure 5.9: Time constant spectra for AlGaN/GaN SBD after a reverse stress voltage (from −50 to −200 V) performed at 4 different temperatures. The inset graph confirms the trap activation energy ∼0.60 eV involved under 4 different stressing conditions.

SBD and TLM structures indicating that the physical location of that trap is within the buffer layer. The bias-dependent R_{ON} increase of AlGaN/GaN SBDs is due to more electron-filling of the E_C−0.60 eV trap in the buffer, which has been confirmed by the observation of an enhanced current transient amplitude for the diode under higher stressing voltages.

5.3.4 Trapping Mechnism in the GET-SBD

To visualize the trap location and understand the trapping phenomena in both SBD and GET-SBD, TCAD simulations have been performed. In the simulator, an acceptor trap at E_C −0.60 eV with uniform spatial density of 10^{17}cm^{-3} (arbitrary number) has been defined in the buffer layer due to C-doped back-barrier.

The electric field distribution in the AlGaN barrier at V_R of −100 V for the conventional SBD and GET-SBD is shown in Figure 5.10 (a) and (b), respectively (also shown in chapter 2). The edge termination in GET-SBD architecture redistributes the electric field and suppresses the peak electric field at the anode edge, thus the leakage current of the GET-SBD is significantly reduced. It should be noted that there is an additional peak electric field at the edge of GET which withstands the voltage in the diode off-state operation. Instead of having a strong electric field peak at the anode edge as in the conventional SBD, two electric field peaks (with lower magnitude) are created in the GET-SBD architecture. According to Poisson's equation (4.4), the integration of the field lines at spatial location gives the electrostatic potential. This can be another perspective to interpret the field distribution in the GET-SBD in Figure 5.10 (b).

As discussed before, the GET-SBD fabricated on a C-doped buffer still shows pronounced R_{ON} degradation though a smoother electric field distribution (shown in Figure 5.10(b)) is realized compared to the conventional SBD. To understand the trapping mechanism, the buffer trap occupancy for the reference SBD and the GET-SBD is shown in Figure 5.10 (c) and (d), respectively. The occupancy of the acceptor states is "0" when it is not filled, and the occupancy equates "1" when an electron is captured by the trap state. The occupancy can be thought of the probability of finding a filled trap. An acceptor atom, when it is filled with an electron, is negatively charged which will deplete the 2DEG. In Figure 5.10 (c), a trapping zone is shown in the buffer layer of the conventional SBD. The location of that trapping region is below the anode edge, which can be caused by the vertical depletion region and the injected electrons inside the buffer due to the presence of a vertical electric field in the depletion region. The filled acceptor, which is negatively charged, depletes the 2DEG and reduces the electron density due to the virtual gate effect [38]. This results in the R_{ON} degradation in AlGaN/GaN SBDs. In the case of the GET-SBD, the electric field peak at the anode edge is lower, which results in a smaller and milder trapping region below the anode edge (shown in Figure 5.10(d)). However, an additional trapping region appears below the GET edge due to the electric field peak at the corner of the edge termination. In Figure 5.10 (e) and (f), the vertical electric field and trap occupation along the y-coordinate at the anode edge of the SBD (location 1), anode edge of the GET-SBD (location 2), and the corner of the edge termination (location 3) are shown, respectively. It can be seen that the field penetrates through the GaN channel into the

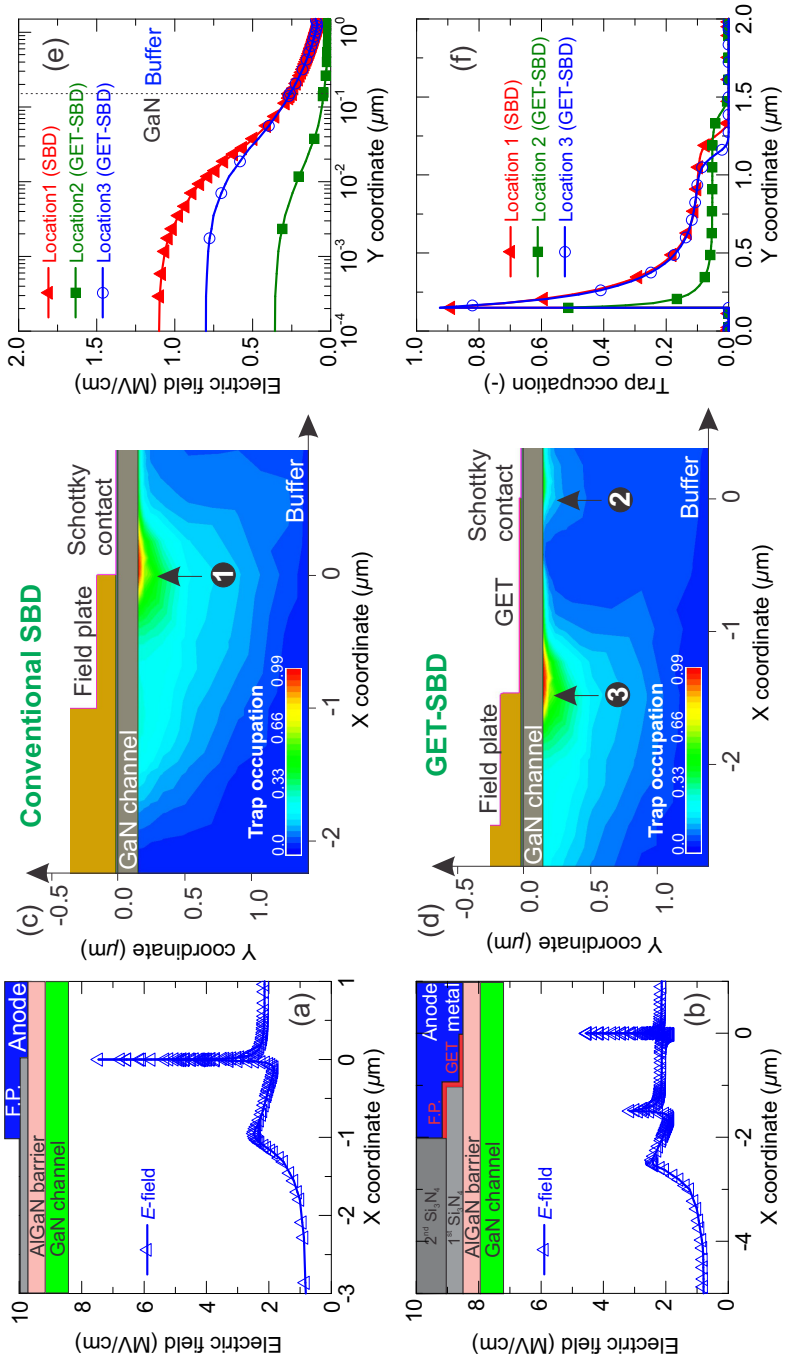


Figure 5.10: The electric field distribution in AlGaN barrier at V_R of −100 V for the conventional AlGaN/GaN SBD (a) and the GET-SBD (b). The buffer trap occupancy at V_R of -100 V for the reference SBD (c) and the GET-SBD (d). (e) The vertical electric field penetration into the GaN channel and buffer layer by taking a vertical cut-line at three different locations as indicated in (c) and (d). (f) The trap occupation in the buffer along the vertical cut-lines.

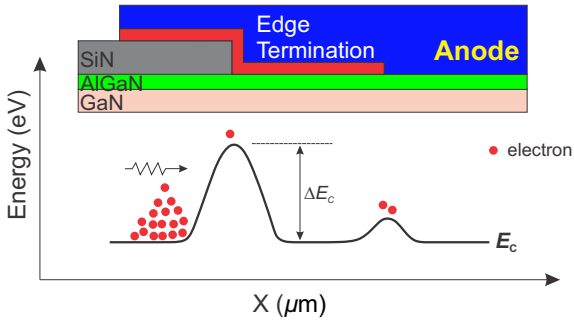


Figure 5.11: Schematic illustration of the energy band in the GaN channel for the stressed GET-SBD. The two increased energy barriers is due to the virtual gate effects of the two trapped regions shown in Figure 5.10(d).

AlGaN back-barrier. The magnitude of the electric field contributes to the 2D trapping regions in the SBD and GET-SBD. In Figure 5.10 (c), (d) and (f), we can observe that the trapping regions in the diodes are non-uniform due to the 2D electric field distribution. From simulated results, we clearly observe an additional trapping region in the buffer layer of the GET-SBD. This explains why the GET-SBD also showed pronounced dynamic R_{ON} increase, though the leakage characteristics were greatly improved. From the results in Figure 5.10, we can conclude that the stability of the GET-SBD can be significantly improved by fabricating the diodes on "trapping-free" buffers, in which case the dominant buffer trapping can be minimized.

In Figure 5.11, a schematic of the conduction band in the GaN channel is shown. After the removal of the stress voltages, the 2DEG will be replenished. However, the 2DEG density is not uniform through the lateral GaN channel. Due to the virtual gate effect from the trapping regions, the 2DEG density is lower in the corresponding channel region. It is important to note that the trapping phenomena and effects are 2-dimensional. Due to the trapping effects, the Fermi-level in the buffer is pinned at the trap level. This results in an increased energy barrier in the channel (shown in Figure 5.11). This gives rise to a non-uniform distribution of the 2DEG in the GaN channel, and the 2DEG density in the region affected by the trapping can be described by:

$$n(E_{C0}, x) = n_0 \times exp(-\Delta E_C / kT), \tag{5.2}$$

where E_{C0}, n_0, ΔE_C are the energy at the conduction band edge, 2DEG density at the access region (free of trapped effects), and the enhanced energy barrier, respectively. During the transient of the 2DEG current, the overall current can be expressed as

$$J_n = -q\mu_n n \nabla \Phi_n. \tag{5.3}$$

The increased energy barrier not only has an impact on the 2DEG density but also can reduce the electron mobility, resulting in a significant increase of the channel resistance (dynamic R_{ON} increase shown in Figure 5.3(b)). This explains why a total current collapse phenomenon occurred in GET-SBD fabricated on a C-doped buffer. The de-trapping kinetics is correlated with the increase of the recoverable 2DEG current by gradually lowering the energy barrier.

From the results in Figure 5.10, we can conclude that the stability of the GET-SBD can be significantly improved by fabricating the diodes on a "trap-free" buffer, in which case the dominant buffer trapping should be minimized.

5.3.5 Stability Improvement by Buffer Design

As has been discussed in sections of this and previous chapters, dynamic R_{ON} stability and the diode leakage current are not necessarily correlated. When the buffer trapping mechanism is dominant, the GET-SBD showed more pronounced R_{ON} increase than the conventional AlGaN/GaN SBD and suffered from total current collapse due to a significant increase of the channel resistance.

To improve the dynamic stability, both surface trapping and buffer trapping should be minimized. Additionally, Croon *et al.* showed that the contribution of buffer trapping can be varied by the substrate connection [112]. Depending on the specific application, the backside substrate should be electrically connected to the non-switching node to reduce electromagnetic interference (EMI) [112]. Based on this, the substrate connection modes for GaN-based Buck and Boost converters are shown in Figure 5.12. In Buck converters, the anode contact node is the stable non-switching node where substrate should be connected. On the contrary, the anode contact in a Boost converter is switching. Thus, it is advised to contact the substrate of the GaN diodes to the non-switching cathode contact. In these two configurations, the potential drop across the buffer is just the opposite. As reported in the work by Croon *et al.*, a substrate-cathode connection (corresponding to the Boost converter case) gives rise to more current collapse of the GaN diode compared to connecting the anode with the backside.

Various buffer designs have been proposed by Stoffels *et al.* to obtain a lower trapping buffers at a high voltage range [90]. The asymmetric buffer trapping characteristics are due to the asymmetric band diagram across the buffer layers. In [90], it was shown that a superlattice-based buffer showed very low buffer trapping when the surface-to-substrate potential is positive. To further confirm that the dynamic stability of GET-SBD can be significantly improved by using a low-trapping buffer, the reported superlattice-based buffer was chosen for the device fabrication [90]. The goal of this section is to demonstrate that the dynamic R_{ON} stability can be improved by proper buffer design. Thus, the pulsed I–V measurements were performed in the way corresponding to the Buck-converter schematic with anode-substrate connection.

In Figure 5.13(a), typical pulsed I–V characteristics of non-recessed GET-SBDs are shown with a pre-bias down to −200 V. The alternative buffer used is a superlattice-

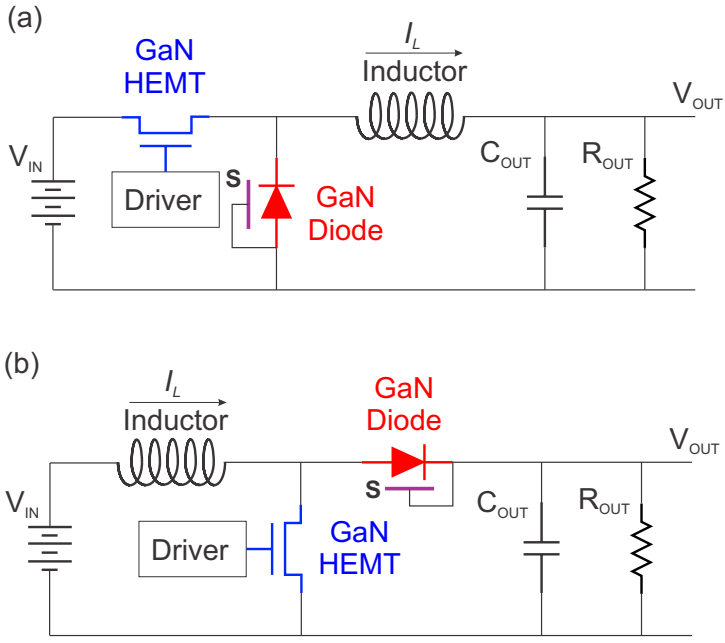


Figure 5.12: The substrate connection in GaN-based Buck converter (a) and Boost converter (b). The "**S**" denotes the substrate node (i.e. silicon wafer) in AlGaN/GaN lateral Schottky diode.

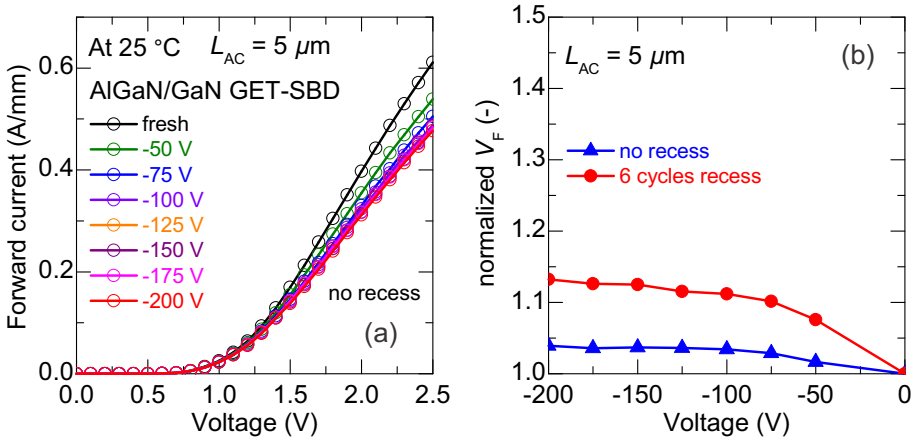


Figure 5.13: (a) Pulsed *I–V* characteristics of AlGaN/GaN GET-SBD with various pre-bias stressing conditions down to −200 V. (b) The normalized forward voltage for GET-SBDs with 2 different AlGaN barrier recess conditions.

based buffer, and the trapping from the buffer is minimized [90].With a pre-bias at −200 V, the GET-SBD shows reasonably good on-state characteristics without exhibiting total current collapse. This validates the previous discussions in this section; furthermore, it provided a solution to obtain both good leakage current and dynamic characteristics for GaN-based diodes. In Figure 5.13(b), the normalized forward voltages with stressing pulse for non-recessed GET-SBDs and recessed GET-SBDs (with 6 cycles ALE) are compared. Both diodes obtained a dynamic forward voltage increase lower than 20% after a pre-bias at −200 V. It is most likely that the residual dynamic forward voltage increase is related to surface-related trapping. From the recess-dependent dynamic characteristics, the trapping mechanism may occur at the anode edge or at the corner of the GET structure, at the Si_3N_4/AlGaN barrier interface due to the presence of electric field peaks.

5.4 Summary and Conclusions

In this chapter, the dynamic stability of AlGaN/GaN conventional SBD and GET-SBD architectures fabricated on a carbon-doped buffer was extensively investigated. The carbon incorporation into the $Al_{0.08}Ga_{0.92}N$ was controlled by precisely tuning the growth temperature in the MOCVD reactor. The GET-SBD, fabricated on a carbon-doped buffer, showed enhanced BV and a suppressed leakage current. However, a total current collapse phenomenon was observed in these GET-SBDs, that is more severe than the dynamic characteristics of the conventional AlGaN/GaN SBDs.

Current transient measurements on the AlGaN/GaN SBD confirm that the dynamic

R_{ON} increase is due to an electron trapping mechanism instead of permanent damage under high-field stress conditions. By simultaneously comparing the trap spectra of AlGaN/GaN SBDs and TLM structures under the same stressing voltage, it has been confirmed that the trapping mechanism is located in the buffer layers. The bias-dependent R_{ON} increase of the AlGaN/GaN SBD is due to more electron-filling of the same buffer trap, which has been confirmed by the observation of an enhanced current transient amplitude for the diode under higher stressing voltages. To understand the total current collapse phenomenon in the GET-SBD under high stressing voltage, a 2-D TCAD simulation has been performed to visualize the trap occupation in the buffer where the extracted trap level was defined. The simulated results showed that the GET-SBD suffered from an additional trapping mechanism below the GET edge due to the capacitive coupling. It also indicates that the dynamic R_{ON} increase is not only dependent on the electric field peaks, but also on the distribution of the electric field.

In the final section, "trap-free" AlGaN/GaN GET-SBDs have been demonstrated by fabricating the diodes on low-trapping AlGaN/GaN buffer layers. On these buffers, the total current collapse phenomenon was not observed, the residual increase of the dynamic R_{ON} and forward voltage is mostly likely contributed by the trapping at the Si_3N_4/AlGaN interface. This gives validation of the analysis in this chapter and demonstrates that high-performance and stable GaN diodes on silicon substrates have been realized.

Chapter 6

Long Term Stability and Reliability of GaN Diodes

In this chapter, ON- and OFF-state accelerated stress tests are reported to evaluate the long term stability and reliability characteristics of high performance GET-SBD devices. The degradation modes under different stress conditions in both ON- and OFF-state have been experimentally investigated. Based on the voltage-acceleration tests, the device lifetime can be evaluated targeting specific voltage applications. The GET-SBD demonstrates good device reliability under ON-state stress. A time-dependent breakdown mechanism in the GET-SBD, under OFF-state stress, can lead to permanent leakage degradation and eventually device failure limiting its high-voltage applications.

6.1 Introduction

To guarantee the success of a technology in the market, the reliability and lifetime requirements for the semiconductor components should be fulfilled. Despite the progressive development of GaN-based power semiconductor devices, only few reliability papers and application notes are available. Recently increasing attention has been received to investigate the degradation mechanisms of GaN power devices under high-temperature, high current (ON-state) or high-voltage (OFF-state) stress conditions [113–115].

Elaborate reliability studies on low-voltage RF GaN HEMTs have been previously studied by many research groups [26, 45, 116]. Permanent damage and failure of the GaN HEMTs can originate from contact degradation [117, 118], AlGaN structural degradation [119–121], electrochemical reaction triggered degradation [122], and vertical buffer breakdown [123], etc. Improvement in GaN HEMT reliability was reported by epi-structure design, field-plate design, proper passivation techniques, etc. [124].

In this chapter, both ON- and OFF-state stress measurements are presented on state-of-the-art GET-SBDs to investigate the degradation modes and extrapolate the lifetime.

6.2 ON-State Stress

This section will show the Measure-Stress-Measure (MSM) procedure which was used to analyze the degradation mechanisms when a large forward current is forced through

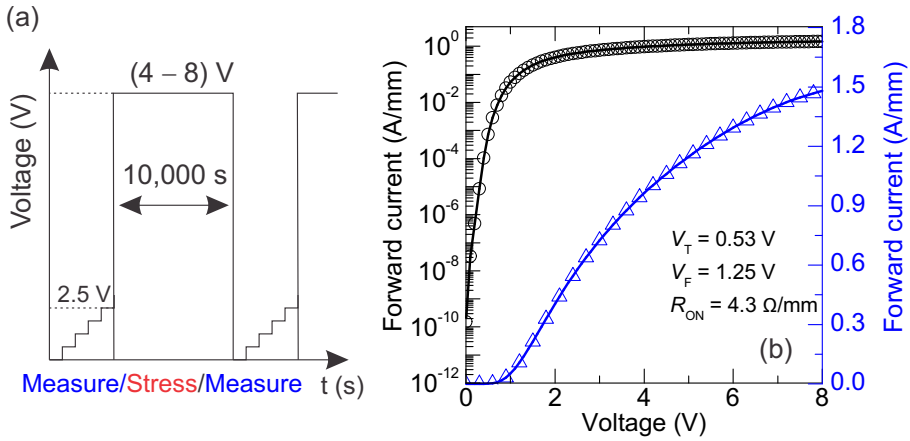


Figure 6.1: (a) Schematic showing the measure/stress/measure technique to evaluate the GET-SBD degradation under ON-state stress. (b) A typical forward characteristic of the GET-SBD under test. The nominal V_T and V_F of the GET-SBDs are 0.53 and 1.25 V, respectively.

the AlGaN/GaN GET-SBDs. We experimentally investigate the impact of forward voltage stress on the main figure of merits, such as turn-on voltage (V_T) and forward voltage (V_F). Stress analyses at different voltages and temperatures are performed and the recovery phase of the same stressed diode, recurring after the removal of the stress voltage, is further monitored. Furthermore, the lifetime extrapolation on the GET-SBD was evaluated under ON-state operation mode proving a good device reliability.

6.2.1 Measurement Procedure

The forward reliability study has been performed by using the conventional measure-stress-measure (MSM) routine shown in Figure 6.1(a). During the stress phase, a constant voltage (stress voltage V_S varying from 4 to 8 V) is applied on the anode contact while short-circuiting the two cathodes with the substrate. The stress phase lasts for 10000 s without interruption. After the stress phase, the stress voltage was removed to monitor the turn-on voltage (V_T) and forward voltage (V_F) variations by measuring a full *I–V* characteristic from 0 to 2.5 V. It is possible that the diodes immediately recover some part after the removal of the stress voltage, some advanced techniques to assess the real degradation before device relaxation can be found in [125,126]. The criteria for the definition of V_T and V_F of the GET-SBD aligns with the ones used in previous chapters. The turn-ON and forward voltages were extrapolated at a normalized current of 1 and 100 mA/mm, respectively.

In Figure 6.1(b), a typical forward *I–V* characteristic (from 0 to 8 V) of the GET-SBD under test is presented. The anode-to-cathode spacing (L_{AC}) of the GET-SBDs is

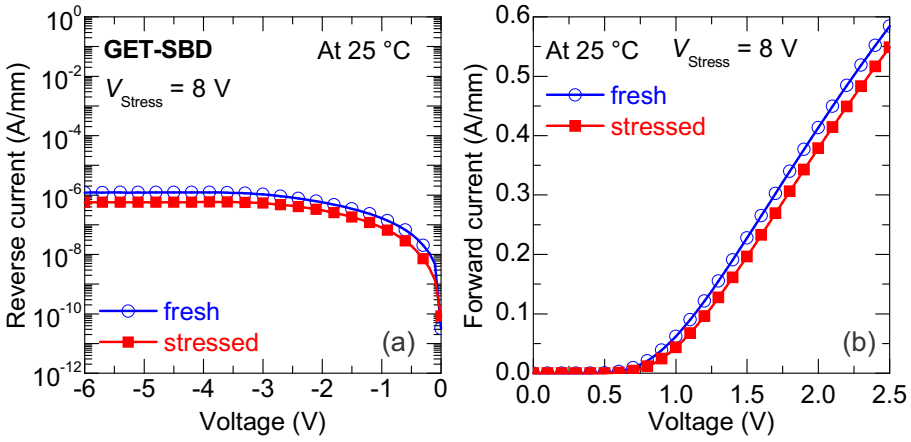


Figure 6.2: The comparison of off-state (a) and on-state (b) characteristics between fresh GET-SBD and the one after on-state stress for 10,000 s.

5 μm. At 25 °C, the median turn-on and forward voltages of the GET-SBDs are 0.53 and 1.25 V, respectively. At the end of the stress phase, the reverse leakage current was evaluated by sweeping anode voltage V_A from 0 and −6 V. The reverse voltage of −6 V was chosen instead of −100 V to avoid additional trapping or damage induced by the high voltage and electric field in off-state. This allows us to focus the study on the diode forward voltage degradation. Finally, the recovery was monitored by applying 0 V (recovery voltage V_R) and periodically analyzing V_T and V_F.

6.2.2 Experimental Results and Discussions

In Figure 6.2(a) and (b), the off-state and on-state characteristics of the fresh GET-SBD and the one after on-state stress for 10,000 s are compared. In this test, the stress voltage was 8 V. It can be observed that the leakage current of the stressed GET-SBD shows a slight decrease. It can be related to some residual trapping effects increasing the energy barrier for electron injection. In the on-state, the stressed GET-SBD shows degradation of the forward voltage (i.e. at a current level at 100 mA/mm). The on-resistance (related to the slope in the linear region) appears to be stable. The forward voltage of the GET-SBD can be related to the turn-on voltage and the on-resistance through following equation:

$$V_F = V_T + R_{ON} \times I_{ON}. \tag{6.1}$$

It shows that turn-on voltage degradation directly leads to an increase of the forward voltage. From the characteristics in Figure 6.2(b), the degraded I–V shows almost parallel shift to the right. To understand this degradation, measurements have been

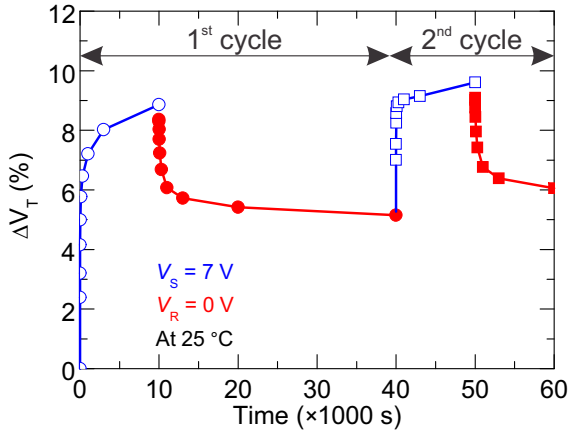


Figure 6.3: Turn-on voltage shift during two cycles of ON-state stress and recovery. The comparison of the stress and recovery phases in two cycles is replotted in logarithmic scale in Figure 6.4.

performed to evaluate the degradation and recovery of the turn-on voltage.

The turn-ON voltage shift occurring during the ON-state stress and recovery (2 cycles of stress and recovery were performed) is shown in Figure 6.3. The stress voltage in this test is 7 V. During the stress phase, electrons are trapped in the region under the anode (Schottky junction) causing an increase in the Schottky barrier height, and hence in V_T. Then, as the stress is removed (recovery phase), some defects are de-trapped and a partial V_T recovery occurs. A second cycle of stress and recovery is performed in order to understand which kind of trapping/detrapping mechanism occurs, by comparing the two stress and recovery dynamics.

In Figure 6.3, the GET-SBD shows a fast V_T increase during stress and partial V_T recovery after stress. After 30000 s, the stressed GET-SBD still did not show complete recovery. The V_T shift in the recovery phase saturates to around 6%. In the second cycle, the V_T shifts more compared to the fresh GET-SBD. This means that additional damage was created. The V_T in the recovery stage of the second cycle saturates as well to around 6%. Based on the results in Figure 6.3, there are two types of degradation mechanisms. The GET-SBD suffers from a permanent damage related to the saturated V_T and a recoverable degradation corresponding to the V_T recovery.

Based on the results in Figure 6.3 and Figure 6.4 regarding the V_T shift and recovery, the following observations can be made:

1. In both degradation cycles (Figure 6.4), the relative degradation occurring during the first 10 s of stress is comparable to the amount of the corresponding subsequent recovery ($\approx$ 4% and $\approx$ 3.2% for the first and second cycles, respectively).

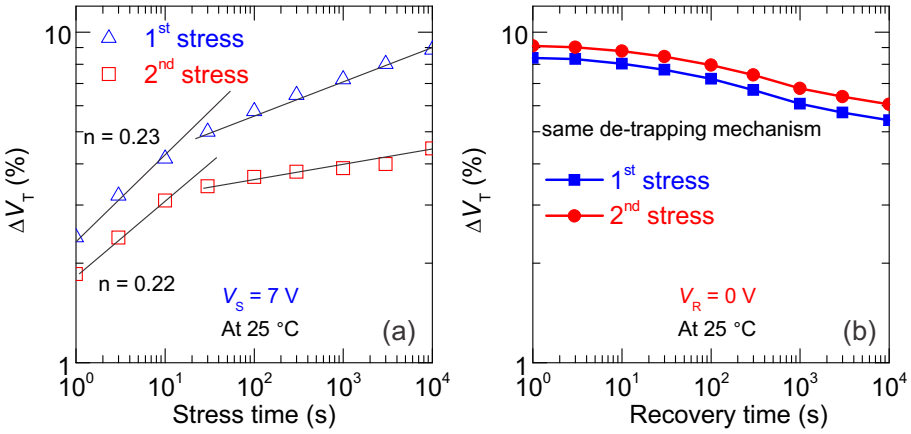


Figure 6.4: The dual slope shown in the stress phase (a) is probably attributed to two different mechanisms, build-up of charges and new trap creation, precisely. V_T degradation related to the second cycle is calculated with respect to the end of the first recovery phase. (b) The two recovery phases show a similar dynamics, meaning that same defects are involved in the de-trapping mechanism.

2. For short stress times (≈10 s), the V_T degradation features the same kinetics (same slope) in both cycles (Figure 6.4(a)).

3. The two recovery phases exhibit the same trend in Figure 6.4(b).

To summarize, by considering together all aspects, we can conclude that the shift of the turn-on voltage in the first 10 s of stress and during the whole recovery phase, in both cycles, may be mainly ascribed to the trapping and de-trapping of the same pre-existing defects. In addition, these results suggest that pre-existing defects are the source of the recoverable degradation component, whereas the new created defects cause a quasi-permanent or slowly recoverable component. The pre-existing and newly created defects may have different physical origin, which results in different slopes in Figure 6.4(a).

6.2.3 Voltage-Dependence and Lifetime Extrapolatioin

As the stress voltages increases, more forward current is forced to pass through the GET-SBD, as is displayed in Figure 6.1(b). Due to the increased power and elevated junction temperature, more severe degradation of the GET-SBD can occur at higher stress voltages and at high temperature conditions.

The voltage dependence of both turn-on and forward voltage degradation can be modeled by a power law, as is shown in Figure 6.5. The slope for the turn-on voltage

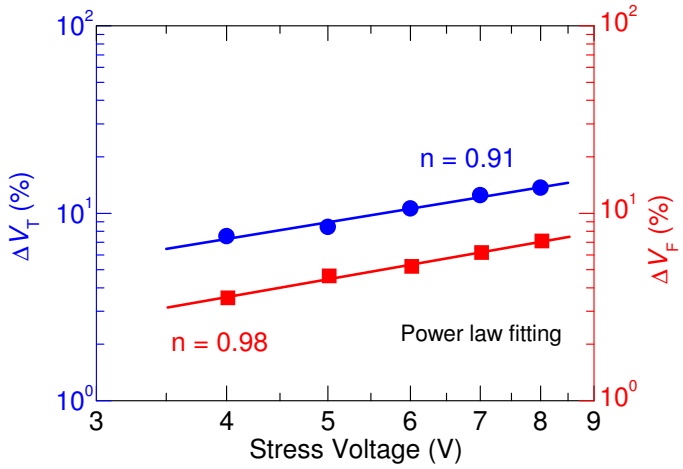


Figure 6.5: Turn-on and forward voltage degradation versus stress voltage. A power dependence is observed for both parameters.

and forward voltage shift is slightly different, which can be due to the contribution of R_{ON} degradation [113] in the forward voltage degradation as shown in the equation 6.1. The analysis of the on-state degradation at different stress bias conditions, by means of the constant voltage-stress method, allowed us to estimate the lifetime of the GET-SBDs at the temperatures of 25 °C and 150 °C in Figure 6.6. The lifetime has been extrapolated by considering the forward voltage degradation since it takes into account both V_T and R_{ON} degradation as described in the equation 6.1.

In Figure 6.6, it is confirmed that more degradation occurs in the GET-SBD when it is stressed at high temperature of 150 °C. At the same stress voltage, the GET-SBD shows a shorter lifetime at 150 °C than at 25 °C, by adopting as a failure criterion a shift of 5% in forward voltage. By using the power law as the lifetime extrapolation model, the maximum applicable voltages to reach 10 years lifetime at temperatures of 25 °C and 150 °C are 1.85 and 1.35 V, respectively for the GET-SBD. For the considered samples, the nominal operating voltages of the GET-SBD at 25 °C and 150 °C are 1.25 V and 1.30 V, respectively. Therefore, we can conclude that the expected lifetime of GET-SBDs reaches more than ten years, operating at both 25 °C and 150 °C.

6.3 Time-Dependent Breakdown under OFF-state Stress

The time-dependent dielectric breakdown (TDDB) mechanism has been extensively studied in the metal-oxide-semiconductor (MOS) system where the insulating gate oxide plays a fundamental role. As the oxide thickness continuously scales down to extreme dimensions for high-performance logic technology, TDDB failure of semiconductor components has become a serious reliability concern. In this section, wide band gap AlGaN/GaN GET-SBDs have been stressed in the off-state at high

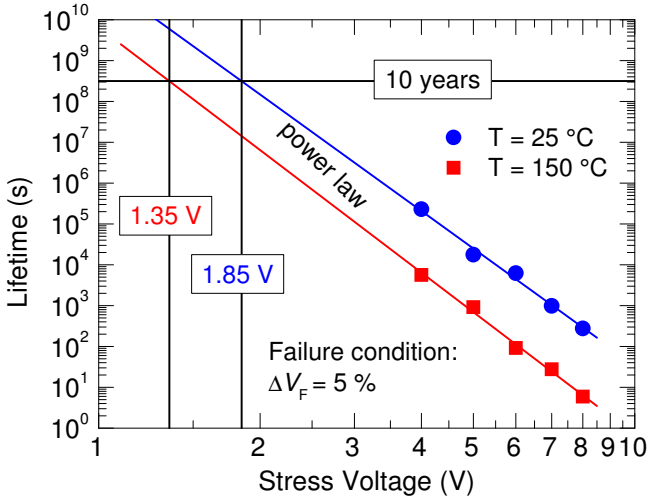


Figure 6.6: Lifetime extrapolation. The failure criterion is considered as a 5% of the forward voltage shift in 10 years at temperature of 25 °C and 150 °C. In the worst case (150 °C), the maximum applicable voltage is higher than nominal operating voltage ($V_F \approx 1.30$ V).

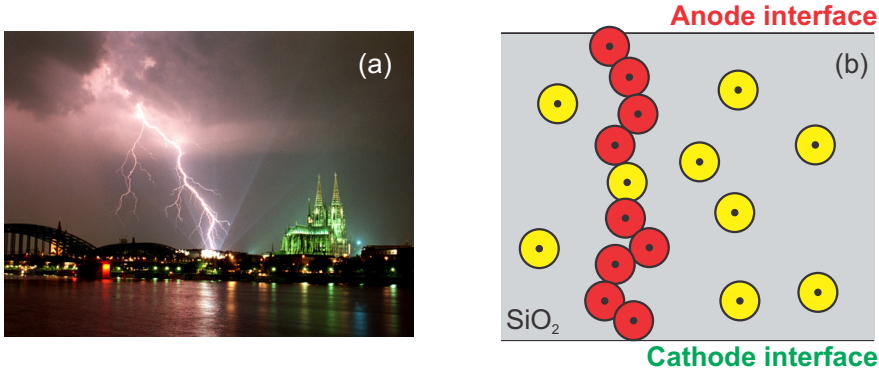


Figure 6.7: (a) A gas-phase (air) breakdown creating a conductive path between a charged cloud and the ground [127]. (b) The illustration of solid-state SiO_2 BD when a conductive path due to generated defects is formed between two electrodes. *Replotted from* [128].

temperature (150 °C) to investigate the stability of the leakage currents and explore the time-dependent breakdown mechanism in the device architecture. A short introduction on the TDDB mechanism in MOSFET technology is discussed first. Statistical evaluation of the TDDB mechanisms in AlGaN/GaN GET-SBDs is performed. TCAD electrical simulations are used to support the hypothesis on the BD mechanisms in GET-SBDs.

6.3.1 TDDB in CMOS Gate Oxides

6.3.1.1 General Background in Dielectric Breakdown

Air and solid state dielectrics (i.e. SiO_2, Si_3N_4, HfO_2, etc.) are insulating materials with a typically large band gap and negligible intrinsic carriers. When the potential across the dielectric is sufficiently high, the electrode-injected electrons can be accelerated by the large electric field leading to a sudden formation of a conductive path in the dielectric. The lightning in Figure 6.7(a) demonstrates a sudden ionization of the air at high electric field conditions to discharge the cloud by creating a short-circuit between a cloud and the ground. A breakdown process of a solid state dielectric is fundamentally similar with the air ionization. In Figure 6.7(b), it shows the threshold moment when a conductive path is being formed between two electrodes in the SiO_2 dielectric.

6.3.1.2 Time-Dependent Mechanism

The fundamental origin of the time-dependent mechanism in dielectric breakdown lies in the random generation of traps within the oxide. When a conduction path is formed

in the oxide, an abrupt increase of the current is typically observed. This percolation model shown in Figure 6.7(b) is commonly used to explain the TDDB phenomena in gate oxide breakdown [128].

To illustrate the progressive gate oxide breakdown, a schematic of different stages of TDDB mechanism is shown in Figure 6.8. The gate of the MOS structure was biased with a constant voltage while monitoring the gate leakage current v.s. stress time (*I*–*t* traces as shown in Figure 6.8(c)). This measurement technique is called "constant voltage test" (CVS), which is widely used for studying TDDB in gate oxide and wide band gap GaN HEMTs [45, 129, 130].

For the fresh silicon based gate dielectric, i.e. SiO_2 and SiON, the defect density is relatively low. Thus, the dominant transport mechanism of the gate leakage (stage "1") is quantum mechanical tunneling of electrons through the energy barrier of the dielectric. During the stress, injected electrons can randomly create traps within the oxide. This leads to an increased gate leakage current due to additional trap-assisted tunneling current. The leakage in stage "2" is typically regarded as stress-induced leakage current (SILC) [131]. When the randomly generated traps form a single conduction path in the oxide, the gate leakage can show a sudden increase in the *I*–*t* trace of Figure 6.8(c). The degraded device undergoes a soft BD (stage "3") with further increase in gate current in Figure 6.8(a). Due to limited heat generation in the stage of soft BD, the device can still be functional [132]. In the following stage of "wear-out" (stage "4"), an increasing number of defects are created. A probability of having the percolation path with more traps is enhancing in stage "4" [129, 133]. As shown in the *I*–*t* trace of Figure 6.8(c), the leakage current becomes more noisy due to electron trapping/de-trapping in the transport processes. This eventually leads to hard BD of the device when a thermal runaway occurs due to localized current flow through the conductive percolation path. The device can show orders of magnitude leakage increase in the *I*–*t* curve. Suddenly the gate dielectric loses completely its insulating properties leading to a device failure [129, 134].

The TDDB failures can be divided into two categories: intrinsic and extrinsic. The mechanism shown in Figure 6.8(a) and (b) corresponds to the intrinsic failure mode of "defect-free" oxides [134]. Extrinsic TDDB mode can be caused by process-induced imperfections (roughness, impurities, structural weakness, etc.). Degraeve *et al.* presented a model for understanding the intrinsic and extrinsic TDDB in MOS structures [135]. A TDDB extrinsic failure can cause an early BD of the device limiting its reliability.

6.3.1.3 Weibull Distribution of TDDB Data

The statistical distribution of time-to-breakdown data in TDDB measurements obeys Weibull statistics which was presented by Weibull in 1951 [136]. In 1983, the Weibull distribution was applied for the first time to examine the statistics of dielectric breakdown and validated by the experimental data [137].

The cumulative density function $F(t)$ of the Weibull distribution is expressed as:

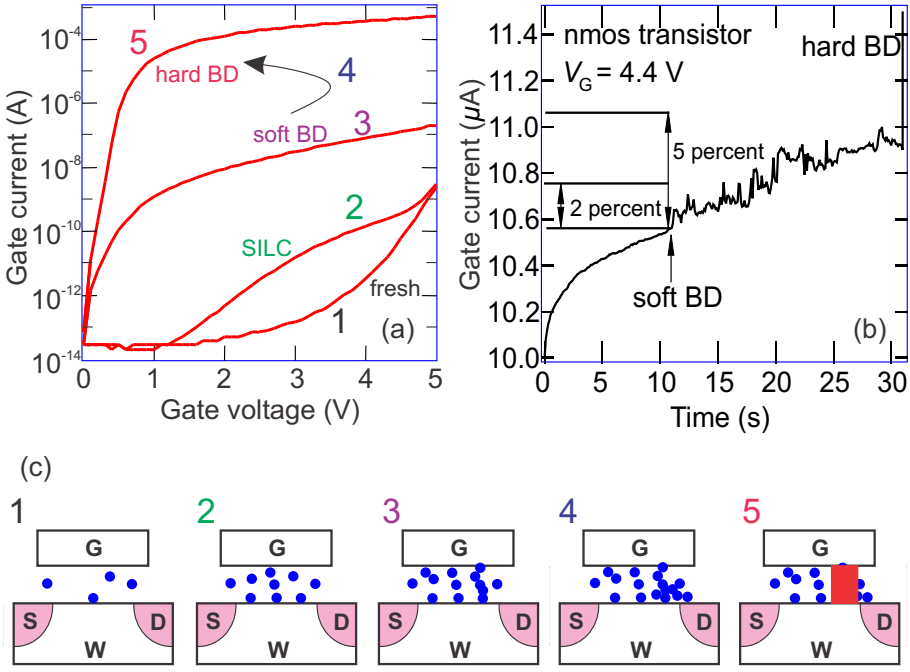


Figure 6.8: (a) An evolution of the gate leakage *I–V* characteristics under constant voltage stress (CVS) test. (b) An example of the gate leakage current during CVS test. (c) A series of schematics showing the random generation of traps within the oxide and a correlation with the gate leakage characteristics. *Courtesy: Prof. G. Groeseneken, Dr. B. Kaczer, imec.*

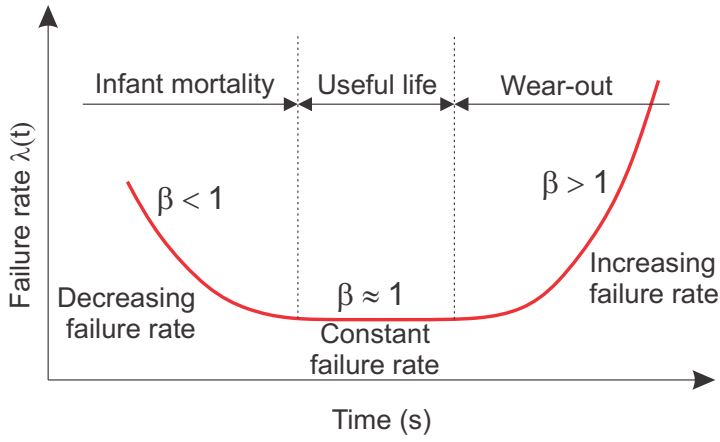


Figure 6.9: The bathtub curve showing three categories.

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right] \tag{6.2}$$

which is equivalent to:

$$\ln\left[-\ln\left[1 - F(t)\right]\right] = \beta \ln(t) - \beta \ln(\eta), \tag{6.3}$$

where β, η are the Weibull slope and the scale parameter or the 63 % value, respectively [129]. The corresponding probability density function $f(t)$ and hazard rate or failure rate $\lambda(t)$ can be calculated below:

$$f(t) = \frac{dF(t)}{dt} = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right], \tag{6.4}$$

$$\lambda(t) = \frac{f(t)}{R(t)} = \frac{f(t)}{1 - F(t)} = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1}, \tag{6.5}$$

respectively.

Depending on the exponent factor β in equation 6.5, the failure rate v.s. time can show a typical bathtub curve depicted in Figure 6.9 with three categories:

1. a decreasing failure rate for $\beta < 1$, mainly due to extrinsic failures (manufacturing defects and structural weakness).
2. a constant failure rate for $\beta = 1$, when failures occur randomly at a constant rate. This corresponds to the useful life of the device with random failure over time.

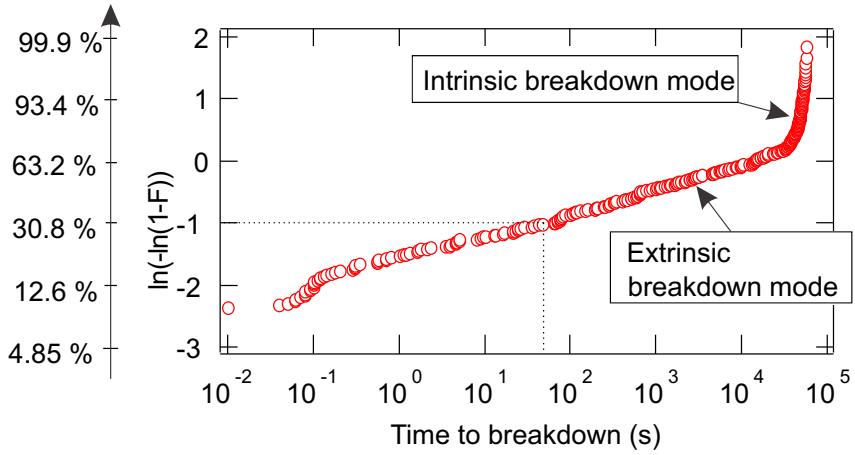


Figure 6.10: Weibull plot of the cumulative density function vs measured t_{BD} values showing two β slopes corresponding to the extrinsic and intrinsic failure modes.

3. an increasing failure rate for $\beta < 1$, this is the "wear-out" region attributed to the accumulated damage and the devices start to fail with increasing frequency.

To estimate the cumulative density function $F(t)$, the measurement data are firstly sorted from smallest to largest and applied with a ranking algorithm [129], using the Benard approximation below:

$$F(i) = \frac{i - 0.3}{n + 0.4} \tag{6.6}$$

where i is the number of the failed device and n is the total number of tested devices.

In Figure 6.10, a Weibull plot of the cumulative density function with the time-to-breakdown t_{BD} of measured devices is shown. According to equation 6.3, the slope of the curve is the Weibull slope. Two distinct slopes appear in Figure 6.10, corresponding to two failure modes. The early failures show a small β Weibull slope due to extrinsic breakdown mode, as is shown in the bathtub curve of Figure 6.9. The defects causing the extrinsic failures are present in the structure before the electric stress starts. They can be related to process-induced damage or localized weak spots of the device. The time-to-breakdown corresponding to extrinsic failures shows a wide spread, i.e. orders of magnitude spread of t_{BD} in Figure 6.10. By comparison, the time-to-breakdown of intrinsic failures shows a narrow distribution with a large β parameter. The t_{BD} of intrinsic failures corresponds to the real lifetime of the device, where the breakdown is induced by electrical stress instead of existing defects or weakness in the device.

6.3.2 TDDB in AlGaN/GaN GET-SBD

The AlGaN/GaN GET-SBD is an architecture based on GaN wide band gap structures with Si_3N_4 insulator as the passivation layer and the material for the fabrication of the edge termination. Generally speaking, the entire epi-stack, AlGaN/GaN heterojunction, passivation layer, buffer layers, can all be regarded as insulators. Under high-voltage off-state stress, catastrophic failure of the diode can happen when the wide band gap materials suddenly lose their insulating properties as the failure of a typical gate oxide in a MOS system, discussed in the previous section. In real circuitry applications, the diode is biased in the off-state for a certain period withstanding a high reverse voltage while blocking the current path. When the diode suddenly fails due to this TDDB mechanism, its leakage blocking capability is gone leading to an eventual dysfunction of the circuit.

In this section, the time-dependent BD mechanisms of the edge terminated AlGaN/GaN-on-Si SBDs are investigated under high temperature reverse bias (HTRB) tests. We propose that the 2 distinct BD mechanisms and permanent leakage increases observed in the reliability tests are related to a sequential BD of the Si_3N_4 at the edge termination and the AlGaN barrier. TCAD electrical simulations with the breakdown path modeled as a narrow metal filament through the Si_3N_4 layer reproduce well the permanent leakage degradation after the first BD phenomenon. The following BD of the AlGaN barrier is attributed to an enhanced electric field at the interface of the metal filament and AlGaN barrier, that has been validated by TCAD simulations. A lifetime extrapolation based on the voltage-dependent TDDB characteristics will be performed at the end of the section.

6.3.2.1 Experimental Details and Device BD in DC

An AlGaN/GaN heterojunction was grown on a 200-mm silicon substrate by metalorganic chemical vapor deposition (MOCVD). The epitaxial structure is composed of 10 nm $Al_{0.25}Ga_{0.75}N$ barrier, a 300-nm GaN channel layer, 1 μm thick C-doped GaN as back-barrier, a superlattice buffer stack, and a 200 nm AlN nucleation layer on p-type Si<111> substrates. The wafer was capped by a 5 nm Si_3N_4 layer grown in the MOCVD chamber and a 140 nm Si_3N_4 layer by means of rapid thermal chemical vapor deposition (RTCVD). Before the fabrication of the edge termination, the Si_3N_4 passivation layer was first removed at the anode area by SF_6 dry etching. A 15-nm Si_3N_4 was then deposited inside the anode trench by means of plasma enhanced atomic layer deposition (PEALD) to form the edge termination. The center region was opened to allow the formation of a Schottky contact by depositing a TiN-based metal stack on the AlGaN barrier. A stack of Ti-based metals was used for the cathode contact formation [29] and annealed at 550 °C. The Schottky contact length (L_{SC}), the anode finger width, and the anode-to-cathode distance (L_{AC}) were 9 μm, 100 μm, and 5 μm, respectively. The length of the edge termination is 1 μm, and there is 1-μm anode metal overhang (F.P.) on the Si_3N_4 passivation layer toward the cathode. A schematic of the edge terminated AlGaN/GaN SBD is shown in Figure 6.11(a). The device structure and epi-stack are based on the optimization study in chapter 3 and chapter 5.

The breakdown and HTRB tests were performed by using a Semiconductor Device

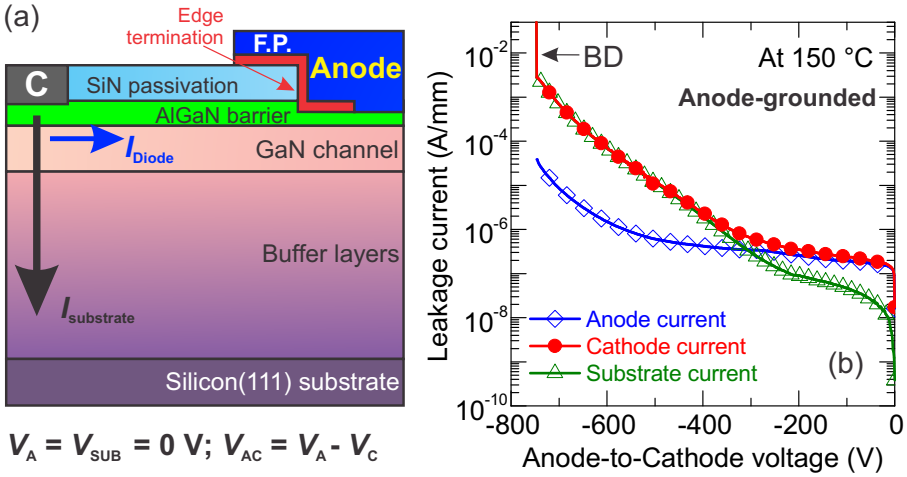


Figure 6.11: (a) A cross-sectional schematic of edge terminated AlGaN/GaN SBD fabricated on silicon substrate. (b) Typical BV characteristics of the diode measured at 150 °C, the anode contact and substrate were biased at ground.

Analyzer (Agilent B1505A). The typical BD characteristics of the edge terminated AlGaN/GaN SBD at 150 °C are shown in Figure 6.11(b). The anode and substrate were biased at ground, while reverse voltage was applied at the cathode contact. The cathode current is the sum of the diode leakage current collected at the anode and the vertical substrate leakage. In Figure 6.11(b), a BV value of ∼ 750 V was reached. When the diode breaks down, it is found that the mechanism was due to the buffer BD.

6.3.2.2 TDDB Mechanisms

The HTRB tests were performed by applying a stress voltage (450, 500, and 550 V) on the cathode while grounding the anode and substrate at a chuck temperature of 150 °C. The time-dependent diode leakage (collected at the anode electrode) and the buffer leakage at the three different stress voltages are presented in Figure 6.12. Under the stressing conditions, the buffer leakage currents are higher than the diode leakage current and show an exponential dependence on the stress voltage. However, the buffer leakage currents are shown to be stable compared to 2 distinct TDDB phenomena (BD1 and BD2) in the diode leakage. This is an indicator of the anode degradation instead of the buffer BD which was the case measured in DC in Figure 6.11(b).

The diode off- and on-state characteristics at fresh condition, after BD1, and after BD2 are displayed in Figure 6.13(a) and (b), respectively. After BD1 mechanism occurs, the leakage current showed ∼2 orders of magnitude permanent degradation. This observation is consistent with the results in Figure 6.12, showing a sudden leakage increase when the BD1 mechanism was triggered. However, the device still functions

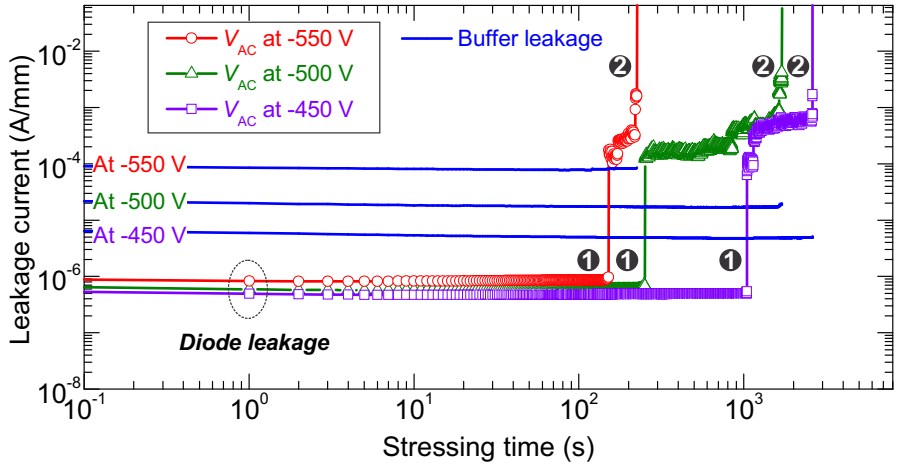


Figure 6.12: Typical time-dependent diode leakage and buffer leakage characteristics at 150 °C under three stressing conditions. The diode leakage currents showed a several-decade jump suggesting the degradation of the anode region.

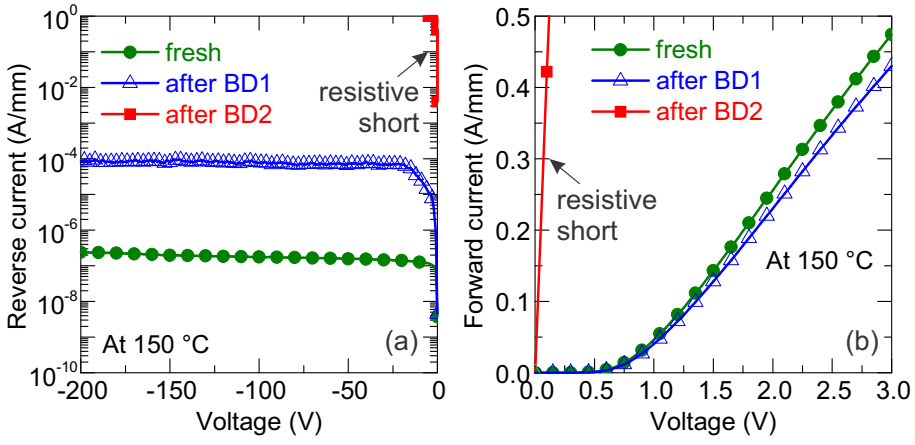


Figure 6.13: The reverse (a) and forward (b) characteristics of a fresh GET-SBD, after BD1, and after BD2.

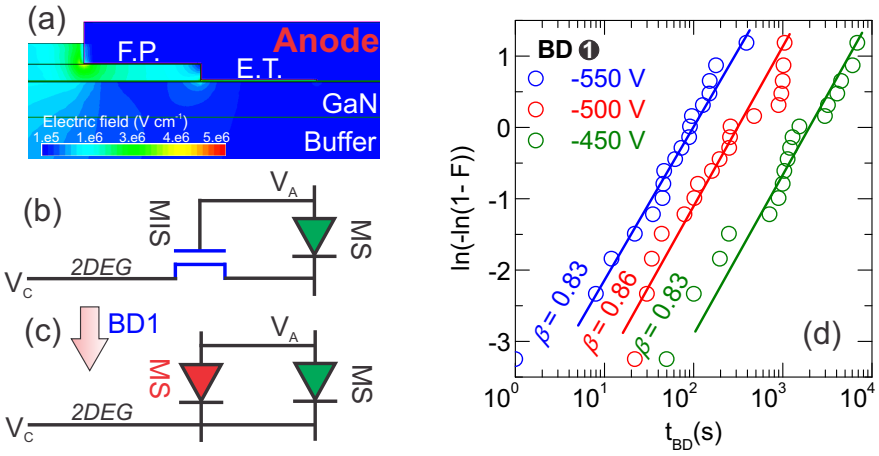


Figure 6.14: (a) The simulated electric field distribution at anode-to-cathode voltage of −200 V. (b) The equivalent circuit of the edge terminated AlGaN/GaN SBD. (c) The proposed circuit model for the diode after BD1 occurs. (d) The Weibull plots of the BD1. Each measurement condition was performed on 18 identical structures.

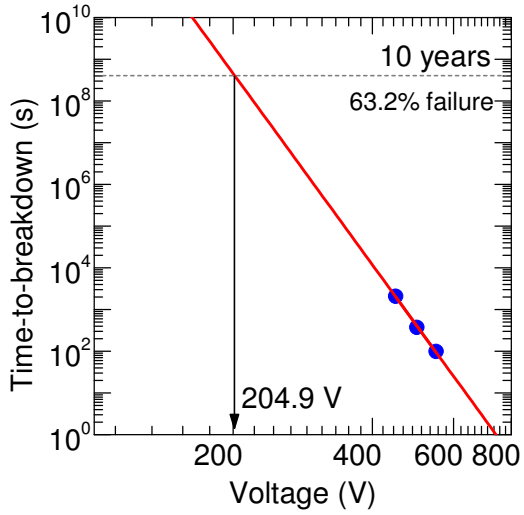


Figure 6.15: The lifetime extrapolation based on the stress voltage accelerated tests. A *Power Law* was adopted.

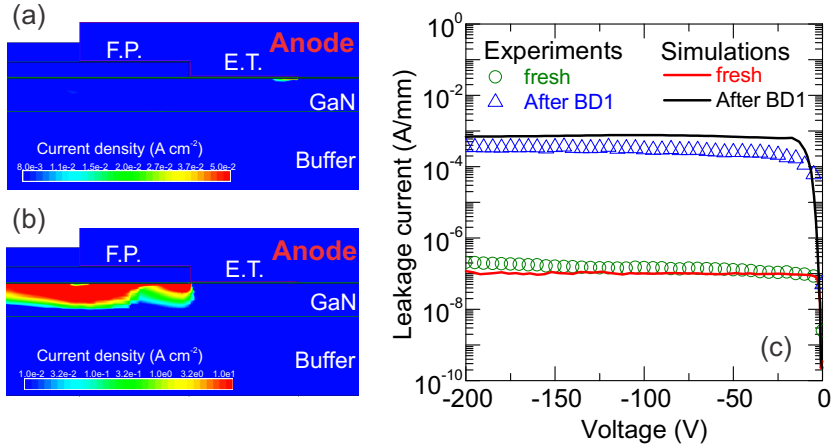


Figure 6.16: The 2-D simulated off-state (at −200 V) leakage currents of the fresh diode and the diode after BD1 are shown in (a) and (b), respectively. (c) Overlay of the simulated and experimental results of the fresh diode and the diode after BD1.

as a diode showing a slightly degraded on-state characteristic in Figure 6.13(b). After the BD2, the diode behaves like a shorted resistor rather than a rectifier, as is shown in Figure 6.13(a) and (b) for both polarities.

To understand these two BD mechanisms, a TCAD structure of the edge terminated AlGaN/GaN SBD was built up allowing for device simulation. In Figure 6.14(a), the simulated electric field (at −200 V) of the anode region is shown. The edge termination can be thought of as a metal/insulator/semiconductor (MIS) structure which allows for the redistribution of the electric field and reduction of the leakage current. The equivalent circuit of the edge terminated AlGaN/GaN SBD is presented in Figure 6.14(b). We propose that the BD1 mode is due to a percolation path formed in the Si_3N_4 of the MIS structure, that results in the transformation of the MIS into a metal/semiconductor (MS) diode structure (shown in Figure 6.14(c)). The malfunction of the edge termination after BD1 leads to a permanent leakage increase and triggers the damage of the AlGaN barrier at the BD2 mode, which has been studied in the Schottky gate GaN HEMT [120].

The Weibull plots of the BD1 examined on 18 structures are shown in Figure 6.14(d). Small β parameters (the slope of the Weibull plots) were obtained in both BD modes, which reflects the nature of an extrinsic BD mechanism. From the electric field distribution in Figure 6.14(a), the field lines are enhanced at the corners of the structure. The non-uniformity of the electric field and the corner shape can be the extrinsic effects causing a low β parameter.

Based on the voltage acceleration TDDB tests, the lifetime of the GET-SBD is extrapolated in Figure 6.15. A 63.2 % of failure percentile was used. The extracted

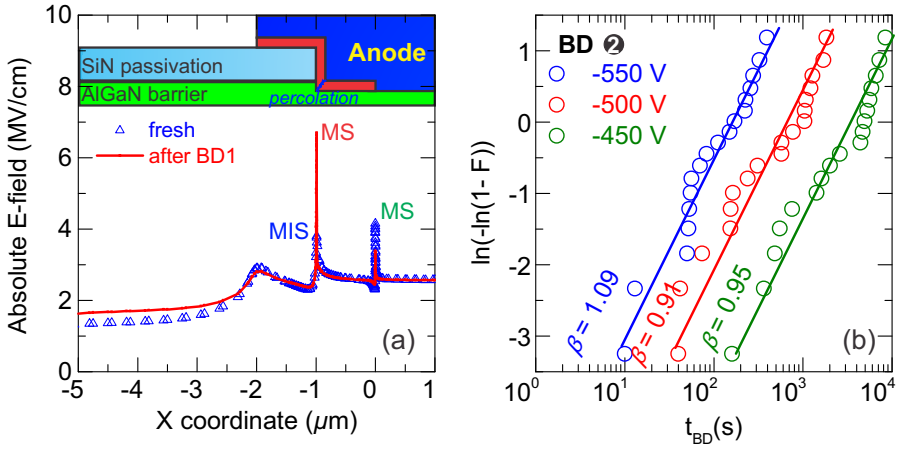


Figure 6.17: (a) The simulated electric field distribution in the AlGaN barrier (0.5-nm away from the MS contact) for the fresh diode and diode after BD1 mechanism occurs. (b) The Weibull plots of the BD2. Each measurement condition was performed on 18 identical structures.

lifetime is shown to be 204.9 V based on the *Power Law* model [138]. In this initial study, the area-scaling effect and 0.01 % of failure percentile were not used for the lifetime extrapolation. However, it also indicates that the TDDB phenomenon in GET-SBDs under long term OFF-state stress can be a reliability issue.

To validate the hypothesis that the corner of the MIS structure was damaged as the BD1 mechanism, a 10-nm wide metal filament was included at the corner of the edge termination [139]. The metal filament was electrically in contact with the AlGaN barrier forming a new MS diode structure at the damaged spot. In this model, we assumed that the barrier height of the new MS diode is the same as the original barrier height of the diode. In Figure 6.16(a), the simulated 2-D leakage currents for the fresh diode and the diode after BD1 are shown. The fresh diode shows very low leakage in the simulation, and the leakage path is located at the MS contact. Before the BD1 mechanism occurs, the leakage through the MIS structure is low though a peak electric field is present at the corner of the edge termination. When the Si_3N_4 as the edge termination breaks down, high leakage currents are shown in Figure 6.16(b) to flow at the new MS (metal filament/AlGaN) diode instead of the fresh MS diode. In Figure 6.16(c), a good overlay of the simulated and experimental leakage currents for the fresh diode and the diode after BD1 is shown.

In Figure 6.17(a), the electric field distribution in the AlGaN barrier (0.5 nm away from the anode contact) for the fresh diode and the diode after BD1 is shown. After a percolation path has formed in the Si_3N_4 as the BD1 mode, an enhanced electric field is observed at the filament/AlGaN interface at the breakdown spot. This results in a

two-orders of magnitude leakage increase. The high electric field (∼7 MV/cm) can promote the second BD mode (i.e. the AlGaN barrier damage) and lead to a permanent damage of the entire structure. The second BD mode is similar to the degradation of the Schottky gate of GaN HEMTs as reported in Ref. [140]. The Weibull plots of the BD2 from 18 repeated structures are shown in Figure 6.17(b).

In summary, sequential TDDB mechanisms in edge terminated AlGaN/GaN SBDs were explained by a proposed model of localized damage of the Si_3N_4 at the edge termination and the AlGaN barrier. The permanent leakage increase of the diode after BD1 is linked with the position of the percolation path, which is modeled as a 10-nm wide metal filament in the Si_3N_4. The simulated results validate the leakage degradation and give a physical explanation of the second BD mode. Avoiding the BD of the edge termination to improve the diode reliability could be possible by using thicker dielectric or other dielectric materials (i.e. HfO_2) and improving the corner rounding process at the anode region.

6.4 Summary and Conclusions

In this chapter, ON-state and OFF-state reliability tests have been performed to extrapolate the lifetime of the GET-SBDs. The voltage-dependent degradation modes have been analyzed extensively in both stressing conditions. The GET-SBD has shown good device reliability under ON-state stress conditions at both 25 °C and 150°C.

Under high temperature reverse bias (HTRB) reliability tests, a sequential TDDB phenomenon in GET-SBDs was demonstrated. Two distinct TDDB mechanisms were observed and are indicative of the anode degradation under high electric field stress conditions, in contrast with the buffer BD measured in DC. The β parameter in the Weibull plots associated with the 2 BD mechanisms is small due to extrinsic failure modes. We propose that the extrinsic breakdown is due to a localized peak electric field at the corner of the edge termination causing a sequential BD of the Si_3N_4 as the material for edge termination and the AlGaN barrier layer. Furthermore, a 2-D TCAD model was built by using a 10-nm wide metal filament through the Si_3N_4 to represent the formed BD path. The simulated electrical results validate our hypothesis that the initial metal/Si_3N_4/AlGaN (MIS) structure degrades into a metal/AlGaN (MS) diode where a high leakage current is flowing through. An enhanced electric field at the new metal/AlGaN junction promotes a sequential BD of the AlGaN barrier and brings about a permanent damage of the entire structure.

The localized damage of the edge termination becomes a reliability concern for the GET-SBD under HTRB tests. In order to improve the diode reliability for higher voltage applications (> 200 V), it is essential to improve the processing-related steps to obtain a high-quality protection layer of the edge termination. Furthermore, the Si_3N_4 is intrinsically defective causing trapping and damage when the device is biased in the off-state. Other dielectric materials (high-k Al_2O_3, HfO_2, etc.) should be explored to improve the off-state reliability maintaining superior blocking capability and leakage characteristics for the GET-SBD.

Chapter 7

Conclusions and Future Perspectives

"*Ars longa, vita brevis*"

High voltage AlGaN/GaN lateral Schottky barrier diodes (SBDs) grown on a silicon substrate have been demonstrated as promising candidates for next-generation high-efficiency power switching applications due to their excellent material properties. Low leakage and low forward voltage of AlGaN/GaN SBDs have been achieved by the combined design of architecture, AlGaN barrier recess, C-doped AlGaN buffer layer, etc. However, the dynamic stability of the diode can be severely influenced by electron trapping effects occurring at the AlGaN surface, (Al)GaN buffer layers, etc., when the diode is subject to a high-voltage stress pulse. The current degradation phenomena of AlGaN/GaN SBD and GET-SBD can be minimized by applying surface cleaning steps, improving the passivation layer and low-trapping buffers. The AlGaN/GaN SBDs with a gated edge termination (GET-SBDs) showed good device reliability under ON-state stress. Under high-temperature reverse bias tests, the GET-SBD showed TDDB characteristics due to localized damage of the Si_3N_4 layer at the corner of the edge termination. The architecture proves to be competitive for 200-V application platform, and further design of buffer and edge termination is required to allow for higher voltage (i.e. 650-V) applications of the diode.

7.1 Conclusions

In chapter 2, the leakage mechanism in conventional AlGaN/GaN SBDs was firstly investigated by temperature-dependent off-state characteristics and TCAD electrical simulations. A high thermally-insensitive leakage current was observed due to a peak electric field present at the anode edge. To reduce the peak electric field and suppress the leakage, two edge terminations were fabricated in AlGaN/GaN SBDs to suppress the leakage currents. It has been confirmed that embedding the edge terminations inside the anode trench (GET-SBD) has a more effective Schottky contact shielding effect than the EET-SBD (the diode with an external edge termination), resulting in a significant drop of the leakage current. A correlation of the simulated electric field in EET-SBD, GET-SBD, and conventional SBD with the leakage current was shown supporting this hypothesis. With the ALE process, a partial removal of the AlGaN barrier at the anode region allows for the improvement of the forward characteristics

without the degradation of the leakage and breakdown characteristics. In this chapter, it has been demonstrated that on-state performance together with a reduced leakage current for AlGaN/GaN diodes can be simultaneously achieved by the design of device architecture and process steps. From the statistical evaluation, the recessed GET-SBDs were proven to be a promising device concept for high-power switching applications. From the breakdown measurements, it was shown that the parasitic vertical leakage through the AlGaN buffer layers (normally unintentionally doped) can dominate the diode overall off-state characteristics when the reverse voltage exceeds ∼300 V. To enable higher voltage applications, a more resistive AlGaN buffer should be designed for the fabrication of AlGaN/GaN diodes.

In chapter 3, the performance of AlGaN/GaN GET-SBDs have been further optimized. To suppress the buffer leakage contribution, a carbon-doped AlGaN buffer was selected due to its lower buffer leakage and higher buffer breakdown voltage than those of unintentionally doped (UID) buffer. With this carbon-doped buffer, the AlGaN/GaN GET-SBDs showed promising reverse characteristics for 200-V applications. The gated edge termination was applied in the AlGaN/GaN SBDs to enable a redistribution of the off-state electric field and a suppression of the leakage current. A further leakage reduction was demonstrated by optimizing the TiN anode metal. The GET-SBDs with IMP TiN showed stronger blocking capability of the leakage than diodes with standard PVD TiN attributed to a higher metal work-function of the IMP TiN. It was also shown that the leakage level is independent of the anode-to-cathode spacing L_{AC} and L_G, which indicates that the edge termination effectively pinches off the 2DEG channel and increases the overall blocking barrier. Moreover, the GET-SBDs with IMP TiN showed high forward currents at 25 °C and 150 °C. Forward modeling showed that a dislocation-assisted tunneling mechanism can be the dominant process for non-recessed SBDs. With AlGaN barrier recessing, direct tunneling and other tunneling mechanisms can be additional processes improving the forward characteristics. To further enhance the on-state performance, the scaling down of the L_G parameter proved to be an effective method without degrading the reverse characteristics. This leads to a reduction of the forward voltage and a more compact device design. This work demonstrates that lateral AlGaN/GaN SBDs with the best performance in terms of low leakage and low forward voltage have been realized in the GET-SBDs in a Au-free technology. Finally, excellent characteristics have been demonstrated on large power diodes with good yield and uniformity (at both 25 °C and 150 °C) on 200-mm silicon substrates and realized by fabrication in a CMOS-compatible process line.

In chapter 4, a pulsed *I–V* measurement procedure was proposed to mimic and characterize the dynamic characteristics of a GaN diode in switching circuits. It allows further trapping analysis of the GaN diodes showing bias-dependent dynamic R_{ON} increases under pulsed *I–V* measurements for both conventional AlGaN/GaN SBDs and GET-SBDs. Besides a gradual current reduction, the GaN diodes also showed total current collapse phenomena and sudden turn-on characteristics. A model of surface electron trapping and Fermi-level pinning was proposed to interpret the data, that has been verified by the current transient measurements and TCAD simulations. Finally, *in-situ* Si_3N_4 grown in a MOCVD chamber has been used as the passivation layer. Due to its growth environment, *in-situ* Si_3N_4 layer typically is denser than RTCVD

Si_3N_4 and contains lower hydrogen. The *in-situ* Si_3N_4 was reported to have ideal Si/N ratio. All this information indicates that the *in-situ* Si_3N_4 can lead to a better interfacial quality of the Si_3N_4/AlGaN interface. From the pulsed *I–V* measurements, it was found that the total current collapse phenomena and Fermi-level pinning effects can be suppressed for AlGaN/GaN SBD with *in-situ* Si_3N_4. It further gives validation of the TCAD model based on the current transient measurements.

In chapter 5, an extensive investigation of the dynamic stability of AlGaN/GaN conventional SBD and GET-SBD architectures fabricated on a carbon-doped buffer has been performed. The carbon incorporation into the $Al_{0.08}Ga_{0.92}N$ was controlled by precisely tuning the growth temperature in the MOCVD reactor. The GET-SBD, fabricated on a carbon-doped buffer, showed enhanced BV and more suppressed leakage current. However, total current collapse phenomena were again observed in these GET-SBDs when the pre-bias reaches −200 V, that is more severe than the dynamic characteristics of the conventional AlGaN/GaN SBDs. Current transient measurements on the AlGaN/GaN SBD confirm that the dynamic R_{ON} increase is due to an electron trapping mechanism instead of permanent damage under high-field stress conditions. By simultaneously comparing the trap spectra of AlGaN/GaN SBDs and TLM structures under the same stressing voltage, it has been confirmed that the trapping is located in the buffer layers. The bias-dependent R_{ON} increase of AlGaN/GaN SBD is due to more electron-filling of the same buffer trap, which has been confirmed by the observation of an enhanced current transient amplitude for the diode under higher stressing voltages. To understand the total current collapse phenomenon in the GET-SBD under high stressing voltage, a 2-D TCAD simulation has been performed to visualize the trap occupation in the buffer where the extracted trap level was defined. The simulated results showed that the GET-SBD suffered from an additional trapping mechanism below the GET edge due to the capacitive coupling. It also indicates that the dynamic R_{ON} increase is not only dependent on the electric field peaks, but also on how the electric field is distributed. In the final section, "trap-free" AlGaN/GaN GET-SBDs have been demonstrated by fabricating the diodes on low-trapping AlGaN/GaN buffer layers. No total current collapse phenomenon was observed, the residual increase of the dynamic R_{ON} and forward voltage is most likely caused by the trapping at the Si_3N_4/AlGaN interface. This gives validation of the analysis in this chapter and demonstrates that high-performance and stable GaN diodes on silicon substrates have been realized.

In chapter 6, ON-state and OFF-state reliability tests have been performed to extrapolate the lifetime of the GET-SBDs. The voltage-dependent degradation modes have been analyzed extensively in both stressing conditions. The GET-SBD has shown good device reliability under ON-state stress conditions at both 25 °C and 150°C. Under high temperature reverse bias (HTRB) reliability tests, a sequential TDDB phenomenon in GET-SBDs has been identified. Two distinct TDDB mechanisms were observed and are indicative of the anode degradation under high electric field stress conditions, in contrast with the buffer BD measured in DC. The β parameter in the Weibull plots associated with the 2 BD mechanisms was found to be small due to extrinsic failure modes. We propose that the extrinsic breakdown is due to a localized peak electric field at the corner of the edge termination causing a sequential BD of the

Si_3N_4 as the material for edge termination and the AlGaN barrier layer. Furthermore, a 2-D TCAD model was built by defining a 10-nm wide metal through the Si_3N_4 as the formed BD path. The simulated electrical results validate our hypothesis that the initial metal/Si_3N_4/AlGaN (MIS) structure degrades into a metal/AlGaN (MS) diode where a high leakage current is flowing through. An enhanced electric field at the new metal/AlGaN junction promotes a sequential BD of the AlGaN barrier and brings about a permanent damage of the entire structure. The localized damage of the edge termination becomes a reliability concern for the GET-SBD under HTRB tests. In order to improve the diode reliability for higher voltage applications (> 200 V), it is essential to improve the processing-related steps to obtain high-quality protection layer of the edge termination. Furthermore, the Si_3N_4 is intrinsically defective causing trapping and damage when the device is biased in the off-state. Other dielectric materials (high-k Al_2O_3, HfO_2, etc.) should be explored to improve the off-state reliability maintaining superior blocking capability and leakage characteristics for the GET-SBD.

7.2 Future Work and Outlook

At the end of this PhD project, some recommendations for future research on the GaN diodes can be put forward.

1. In this work, the combination of the edge termination and AlGaN barrier process in AlGaN/GaN SBDs proves to be effective in obtaining high-performance GaN diodes. The impact of barrier recess on the electron trapping and device reliability due to ON- and OFF-state stress of the GET-SBD should be investigated extensively. The interfacial properties at AlGaN/Si_3N_4 junction have been crucial for the GaN MISHEMT. It is possible that the ALE process can introduce traps at the AlGaN surface and create statistical variation of the AlGaN barrier thickness. This can cause device variation and lead to instability of the barrier height and on-resistance of the GaN diodes under stressing conditions. Future work is required to study the long term stability and reliability of the recessed AlGaN/GaN SBDs.

2. The UID buffer was showing high vertical leakage current limiting the high-voltage applications of the GaN diodes. This phenomenon is commonly understood and related to the unintentional n-type conductivity of (Al)GaN layers. Typically Carbon-doped buffer layers were used to increase the buffer resistivity. However, it brings about severe buffer trapping and dynamic R_{ON} increase. It is of great importance to develop new techniques to obtain a low-trapping buffer while maintaining high resistivity, from the band-diagram point of view. This can give fundamental understanding of parasitive leakage current in the buffer layers.

3. By far, Si_3N_4 is the material used for the fabrication of the edge termination. That layer is crucial since a high electric field is present. However, amorphous Si_3N_4 is reported to be a trapping material intrinsically and widely used in memory technologies [141]. The traps in Si_3N_4 can cause additional leakage

through the edge termination. When a percolation path is formed, it leads eventually to a failure of the diode. Other dielectric materials (poly-AlN, HfO_2, etc.) can be promising to be used as the edge termination due to better bulk properties [142, 143].

4. Lateral field effect rectifier (L-FER) based on enhancement-mode GaN FET was reported demonstrating high-performance rectifying characteristics [144]. There are limited data on the comparison of the DC and dynamic characteristics between L-FER and GaN diodes. It can be important to know which device can be more interesting to be used in a converter circuitry in terms of efficiency, stability, and reliability.

Finally, device-level understanding and performance optimization have been the focus of the thesis. Circuit-based demonstration with GaN power diodes and power transistors has not been performed. As the technologies become more and more mature, research toward real applications should be receiving more attention. The conclusion can be drawn that epi-related issues become limiting factors for high-voltage (650-V) applications. A closer collaboration between epitaxial engineers and device designers should be established to tackle the challenging issues due to early device breakdown, trapping-related instability, and reliability. Continued development and innovation will be needed to push further the potential of GaN technology for high-power applications.

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List of Publications and Awards

Awards and Honors

- Best Oral Presentation at MTL Annual Research Conference, MIT, USA, 2016
- Fellowship for Long Term Research Stay, FWO, Belgium, 2015
- Master degree with *magna cum laude* (rank 1st in the English Master Program), KU Leuven, Belgium, 2012

Patent Applications

1. **J. Hu**. A Group III–N Lateral Schottky Barrier Diode and Method for Manufacturing Thereof, European Patent Application (15197325.2-1552), *submitted and pending*.
2. **J. Hu**. Group III–N Lateral Schottky Barrier Diode and Method for Manufacturing Thereof. U.S. Patent Application (14/757,679), *submitted and pending*.

Journal Papers

1. **J. Hu**, S. Stoffels, S. Lenci, B. De Jaeger, N. Ronchi, A. N. Tallarico, D. Wellekens, S. You, B. Bakeroot, G. Groeseneken, and S. Decoutere, "Statistical analysis of the impact of anode recess on the electrical characteristics of AlGaN/GaN Schottky diodes with gated edge termination," *IEEE Transactions on Electron Devices*, accepted.
2. **J. Hu**, S. Stoffels, M. Zhao, X. Li, A. N. Tallarico, B. De Jaeger, S. Decoutere, and G. Groeseneken, "Enhanced breakdown strength of MOCVD Si_3N_4 as gate dielectric in AlGaN/GaN MISHEMT," *IEEE Electron Device Letters*, to be submitted.
3. **J. Hu**, S. Stoffels, S. Lenci, N. Ronchi, X. Kang, G. Groeseneken, and S. Decoutere, "Time dependent breakdown mechanisms in AlGaN/GaN Schottky barrier diodes with gated edge termination under HTRB test," *IEEE Electron Device Letters*, to be submitted.
4. **J. Hu**, S. Stoffels, S. Lenci, B. Bakeroot, B. De Jaeger, M. Van Hove, N. Ronchi, R. Venegas, H. Liang, G. Groeseneken, and S. Decoutere, "Performance optimization of Au-free lateral AlGaN/GaN Schottky barrier diode with gated edge termination on 200-mm silicon substrate," *IEEE Transactions on Electron Devices*, vol. 63, no. 3, pp. 997–1004, Mar. 2016.

5. **J. Hu**, S. Stoffels, S. Lenci, G. Groeseneken, and S. Decoutere, "On the identification of buffer trapping for bias-dependent R_{ON} instability of AlGaN/GaN Schottky barrier diode with AlGaN:C back barrier," *IEEE Electron Device Letters*, vol. 37, no. 3, pp. 310–313, Mar. 2016.

6. **J. Hu**, S. Stoffels, S. Lenci, S. You, B. Bakeroot, N. Ronchi, R. Venegas, G. Groeseneken, and S. Decoutere, "Leakage and trapping characteristics in Au-free AlGaN/GaN Schottky barrier diodes fabricated on C-doped buffer layers," *Physica Status Solidi (a)*, vol. 213, no. 5, pp. 1229–1235, May 2016.

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8. **J. Hu**, S. Stoffels, S. Lenci, T.-L. Wu, N. Ronchi, S. You, B. Bakeroot, G. Groeseneken, and S. Decoutere, "Investigation of constant voltage off-state stress on Au-free AlGaN/GaN Schottky barrier diode," *Japanese Journal of Applied Physics*, vol. 54, no. 4S, pp. 04DF07, Mar. 2015.

9. **J. Hu**, S. Stoffels, S. Lenci, N. Ronchi, R. Venegas, S. You, B. Bakeroot, G. Groeseneken, and S. Decoutere, "Physical origin of current collapse in Au-free AlGaN/GaN Schottky barrier diodes," *Microelectronics Reliability*, vol. 54, no. 9–10, pp. 2196–2199, Sep.–Oct. 2014.

10. **J. Hu**, S. Lenci, S. Stoffels, B. De Jaeger, G. Groeseneken, and S. Decoutere, "Leakage-current reduction and improved on-state performance of Au-free AlGaN /GaN-on-Si Schottky diode by embedding the edge terminations in the anode region," *Physica Status Solidi (c)*, vol. 11, no. 3–4, pp. 862–865, Apr. 2014.

11. A. N. Tallarico, S. Stoffels, P. Magnono, **J. Hu**, S. Lenci, D. Marcon, E. Sangiogi, C. Fiegna, and S. Decoutere, "Reliability of Au-free AlGaN/GaN-on-Silicon Schottky barrier diodes under on-state stress," *IEEE Transactions on Electron Devices*, vol. 63, no. 2, pp. 723–730, Feb. 2016.

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13. N. Ronchi, B. De Jaeger, M. Van Hove, R. Roelofs, T.-L. Wu, **J. Hu**, X. Kang, and S. Decoutere, "Combined plasma-enhanced-atomic-layer-deposition gate dielectric and in situ SiN cap layer for reduced threshold voltage shift and dynamic ON-resistance dispersion of AlGaN/GaN high electron mobility transistors on 200 mm Si substrates," *Japanese Journal of Applied Physics*, vol. 54, no. 4S, pp. 04DF02, Feb. 2015.

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Conference Contributions

1. **J. Hu**, S. Stoffels, S. Lenci, N. Ronchi, B. De Jaeger, G. Groeseneken, and S. Decoutere, "Impact of AlGaN barrier recess on the leakage and trapping characteristics of AlGaN/GaN Schottky barrier diodes with gated edge termination," in *Compound Semiconductor Week*, Toyama, Japan, Jun. 26–30, 2016.

2. **J. Hu**, S. Stoffels, S. Lenci, S. Decoutere, G. Groeseneken, and T. Palacios, "High performance and stable Au-free AlGaN/GaN lateral power diode on 200-mm silicon substrate," in *MTL Annual Research Conference, MIT*, Bretton Woods, USA, Jan. 20–21, 2016.

3. **J. Hu**, S. Stoffels, S. Lenci, S. You, B. Bakeroot, N. Ronchi, R. Venegas, G. Groeseneken, and S. Decoutere, "Investigation of trapping effects on Au-free AlGaN/GaN Schottky diodes fabricated on C-doped buffer layers," in *11th International Conference on Nitride Semiconductors - ICNS*, Aug. 30–Sep. 4, 2015.

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9. N. Ronchi, B. Bakeroot, S. You, **J. Hu**, S. Stoffels, and S. Decoutere, "Optimization of the source field-plate design for low dynamic $R_{\text{DS-ON}}$ dispersion of AlGaN/GaN MIS-HEMTs," in *Compound Semiconductor Week*, Toyama, Japan, Jun. 26–30, 2016.

10. A. N. Tallarico, P. Magnone, S. Stoffels, S. Lenci, **J. Hu**, D. Marcon, E. Sangiogi, S. Decoutere, and C. Fiegna, "Understanding the degradation sources under ON-state stress in AlGaN/GaN-on-Si SBD: investigation of the Anode-Cathode spacing length dependence," in *IEEE International Reliability Physics Symposium - IRPS*, 2016, pp. 4A-5-1–CD-5-6.

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Curriculum Vitae

Jie Hu was born in Xiangtan, Hunan, P.R. China, on December 18, 1986. He received the B.S. degree in Material Science and Engineering from the Tongji University, Shanghai, P.R. China, in 2010. He received the M.S. degree (*magna cum laude*) in Nanoscience and Nanotechnology from the KU Leuven, Belgium, in 2012. His master thesis was on Electron States in $CuInGaSe_2$-Based Solar Cells: Fundamental Bands and Defect States in Nano-Structured Layers under the guidance of Prof. Valeri Afanas'ev. Since 2012, he has been working towards a Ph.D. degree under the supervision of Prof. Guido Groesekenen at the Department of Electrical Engineering (ESAT), Microelectronics and Sensors (MICAS) of the KU Leuven, Belgium and the group of Power and Mixed Signal Technologies (PMST) at imec, Leuven, Belgium. The main topic of his work was the design of high-performance and reliable integrated GaN diodes for power switching applications. In 2015 and 2016, he was a visiting researcher at Massachusetts Institute of Technology (MIT), Cambridge, Massachusetts, under the guidance of Prof. Tomás Palacios. At MIT, he collaborated to the design of vertical GaN-based devices for power applications through TCAD process and electrical simulations. He has authored or co-authored approximately 30 technical papers for publication in international journals and presentations at conferences.

In 2013–2015 academic years, he was the Ombudsperson for Master of Nanoscience and Nanotechnology at KU Leuven . He served as the president of "Chinese Students and Scholars' Association of Leuven (CSAL)" in 2014–2015.

Jie Hu was awarded the "Fellowship for Long Research Stay" from National Fund for Scientific Research (FWO) of Belgium to perform research at MIT. In 2016, he received the award of "Best Pitch Presentation" at MTL Annual Research Conference, MIT.

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